A CAHNERS PUBLICATION
INTERNATIONAL EDITION
MAY 15, 1986

# EDN

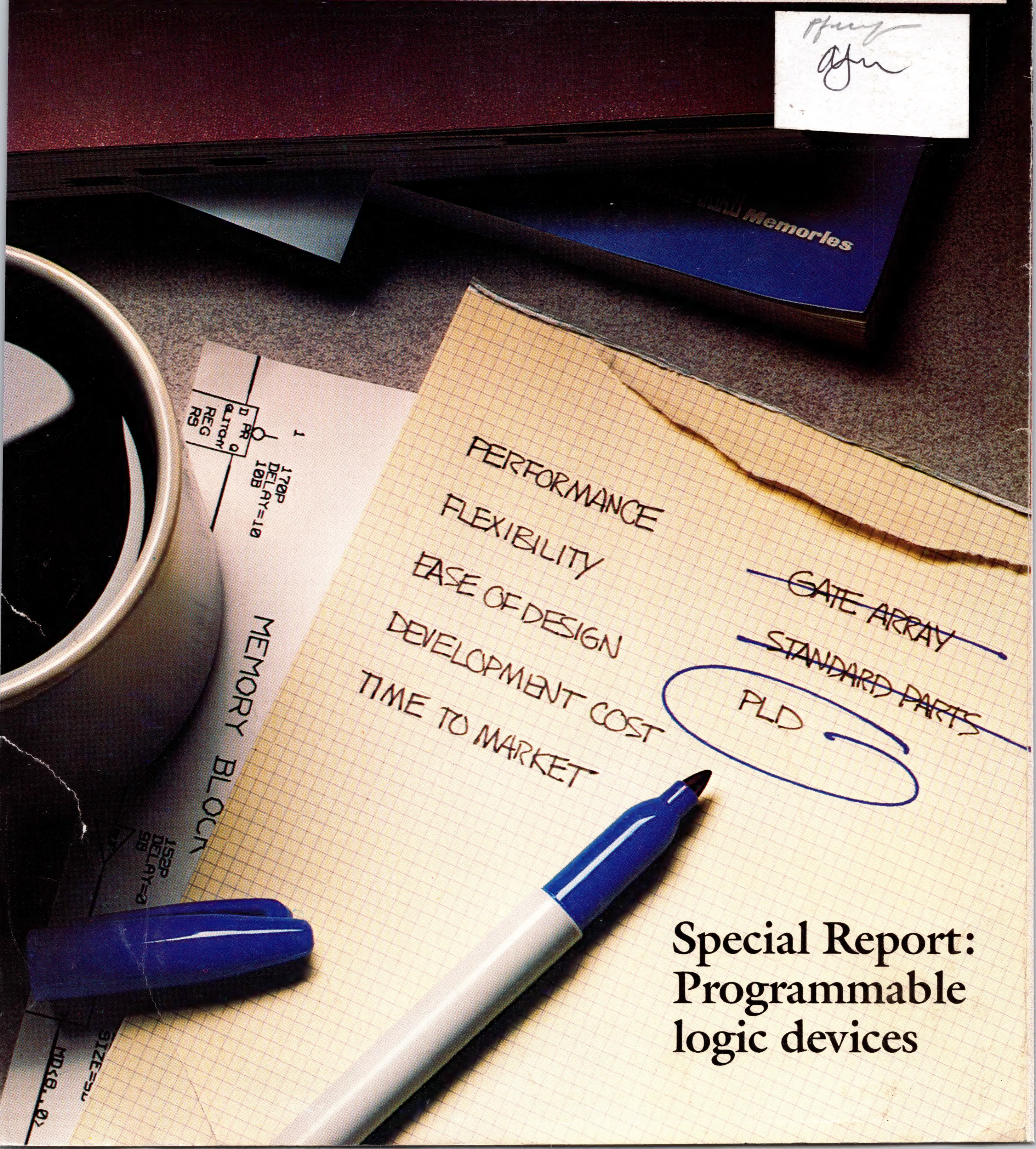
Single-chip op amp delivers ±10A at ±35V

Placement & routing scheme speeds design of VLSI chips

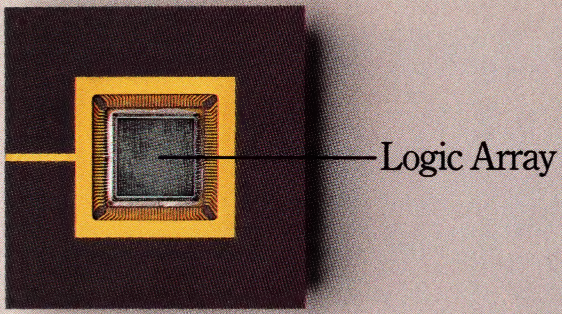
Use a personal computer to generate analog signals

Area-scan image sensors

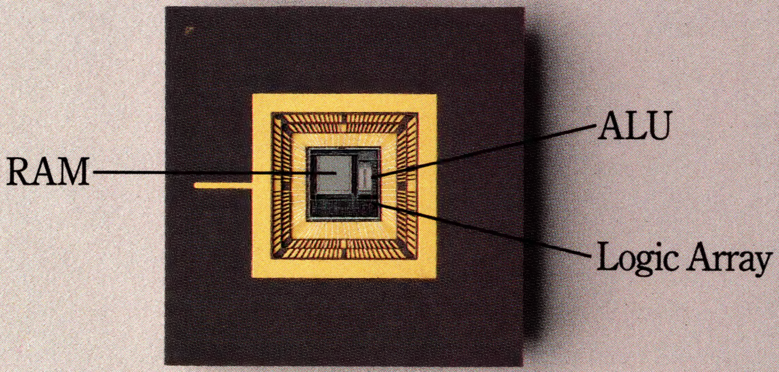
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS




## Special Report: Programmable logic devices




Current Logic

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It's a quantum leap beyond current logic.

It gives you all the advantages of full custom with the ease of a gate array.

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It defies logic. But it makes perfect sense.

LSA2000 Structured Array Family

| Masterslice | Logic Gates | Memory | Logic Megacells |
|---|---|---|---|
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| LSA2002 | 6000 | 3-port 2304 RAM | |
| LSA2003 | 6900 | 4608 RAM | |
| LSA2004 | 5600 | 9216 RAM | |
| LSA2005 | 3700 | 32K ROM | Four 2901s |
| LSA2006 | 3000 | 64K ROM | Eight 2901s |
| LSA2007 | 5000 | 4608 RAM | 16x16 MAC |
| LSA2008 | 5000 | | Two 16x16 MACs |
| LSA2009 | 4500 | 11,520 RAM | |
| LSA2010 | 3200 | 2304 RAM/ 64K ROM | |
| LSA2011 | 5000 | | 16x16 MAC Four 2901s |

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**CIRCLE NO 7**

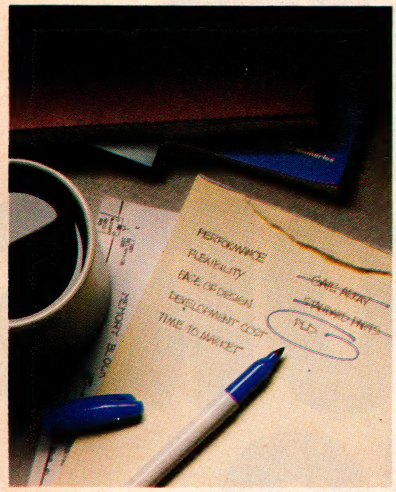
# A BREAKTHROUGH THAT DEFIES ALL LOGIC.

Volume 31, Number 10

# EDN

May 15, 1986

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



***On the cover:** When you evaluate programmable logic devices, you'll find that their advanced architectures are making them suitable for use in state machines and other highly sequential circuits. Indeed, within the past two years, bipolar PLD operating speeds have doubled, and new CMOS PLDs provide four times more circuitry per chip than older bipolar versions offered. See pg 94. (Photo courtesy Monolithic Memories)*

## DESIGN FEATURES



*Continued on page 7*

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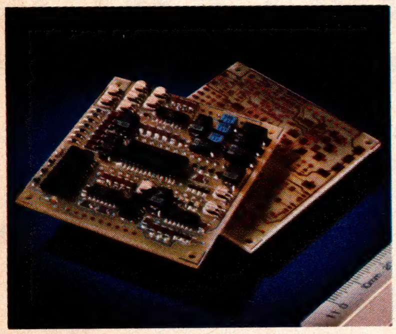

***Solid-state area-scan image sensors** operate on low voltages, come in rugged DIPs, and survive for long periods without requiring realignment. Therefore, they're preferable to vidicon-tube sensors in industrial environments. Nevertheless, the devices must incorporate on-chip scanning logic, which limits your flexibility in controlling the image-scanning process (pg 55).*

## TECHNOLOGY UPDATE



A solid-state area-scan image sensor requires that you add little more than a lens and a few ICs to create a computer system with vision capabilities. These sensors compare favorably with line-scan types and TV vidicon tubes, but choosing the right area-scan image sensors for your application may involve a tradeoff between a variety of factors.—*Peter Harold, European Editor*

## PRODUCT UPDATE



## DESIGN IDEAS



*Continued on page 9*

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*Promotional discount equals the value of the HP 2225A ThinkJet Printer. Offer subject to local conditions.
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CIRCLE NO 94

EI15603

*Continued from page 7*

# EDN

May 15, 1986

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**Managing Editor**
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**Assistant Managing Editor**
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In the rush to create memorable product names and catchy acronyms, electronics companies sometimes misuse and abuse the terminology that we depend on to clarify abstruse technical concepts. No term is more misused than "application specific," usually as used in application-specific integrated circuit, or ASIC.

## NEW PRODUCTS



## PROFESSIONAL ISSUES 271

Women in engineering serve as role models to fight image of male-dominated profession.—*Deborah Asbrand, Staff Editor*

## LOOKING AHEAD 285

Pressure-transducer demand continues rapid growth . . . Demands catch technology in computer-graphics market.

## DEPARTMENTS

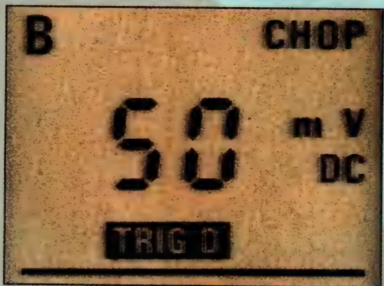


BPA ABP
**Cahners Publishing Company** ☐ Publishers of specialized business publications in Building & Construction ☐ Electronics & Computers ☐ Foodservice ☐ Manufacturing ☐ Medical/Health Care ☐

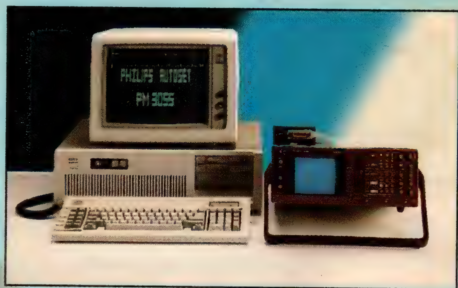
# PHILIPS THE SMART


The new face of 50 MHz 'scope technology

**Advanced-design CRT.** Philips' world-leading know-how in display and monitor tubes ensures optimum brilliance and spot quality. A 16 kV acceleration voltage and advanced electron optics give you display performance you've never seen before in this price class.




**Versatile triggering functions up to 100 MHz.** The PM 3050 family 'scopes have all the regular functions of auto, manual and single-shot triggering, plus smart, secure microcomputer control that 'thinks for you' in auto-triggering mode. Trigger bandwidth is an unmatched 100 MHz.

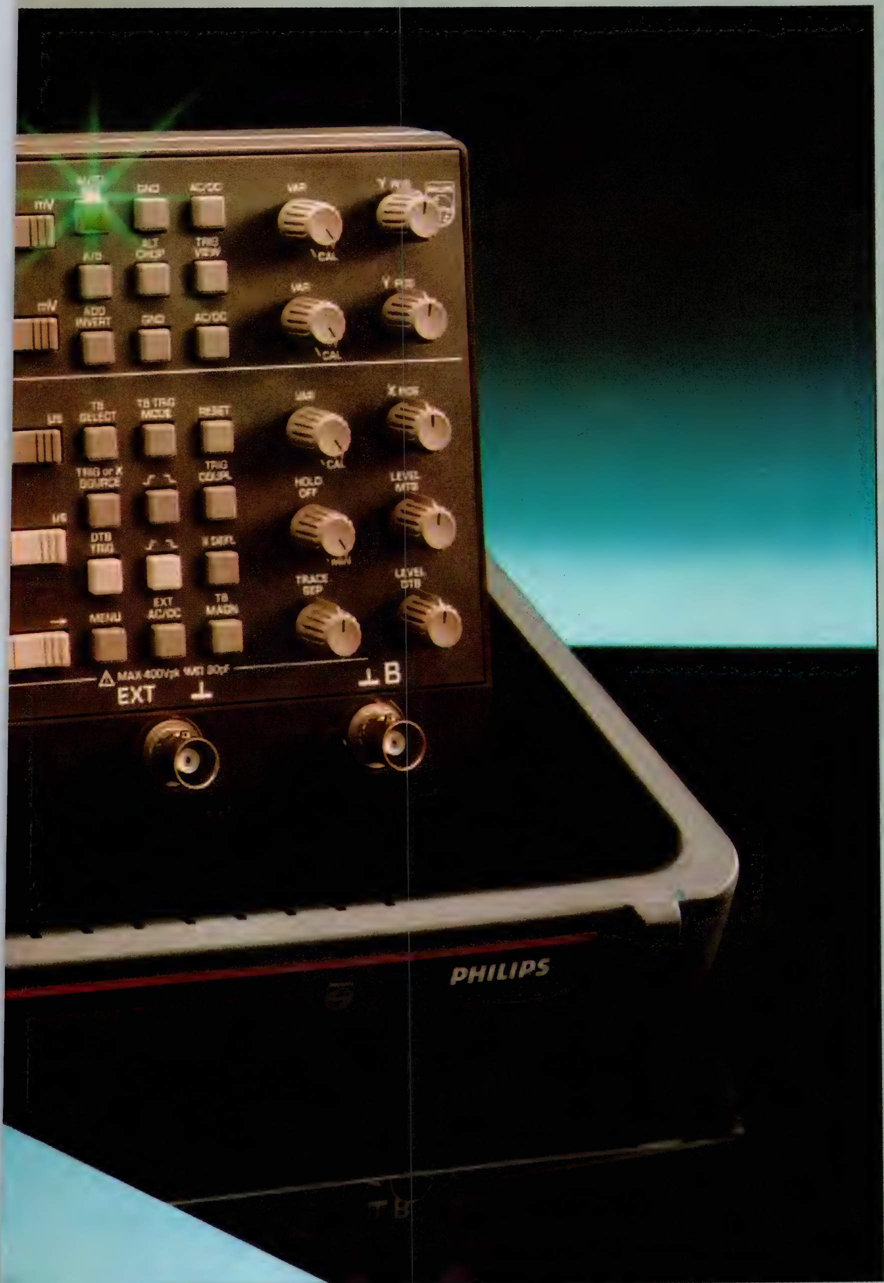


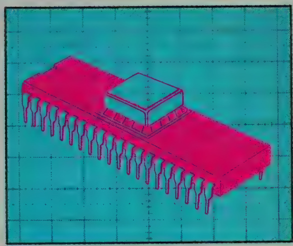

**Fast computer hook-up.** An add-on IEEE-bus option provides fast hook-up to a computer or controller, for use in ATE environments, quality control systems, training and many more applications. The ingenious separate IEEE option is readily interchangeable for automated scope calibration.

# SCOPE

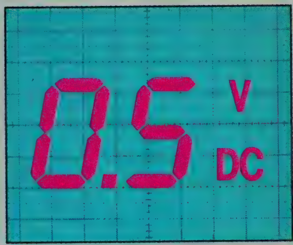
Now, Philips' new technology in 50 MHz 'scopes puts the exciting PM 3050 family way out in front of the world's toughest competition.

For the first time ever in this price range, Philips PM 3050 uses the electronics and manufacturing technologies of the 1990s to take a giant step forward in ease of use and cost-effectiveness.

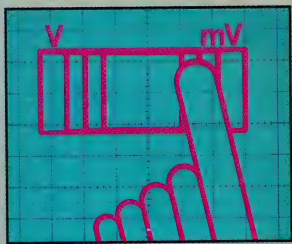


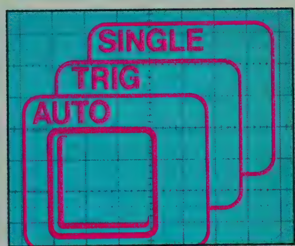
**Autoset.** PM 3050's green button gives you instant, fully automatic setting of all scope parameters – amplitude, timebase and triggering – for any input signal.



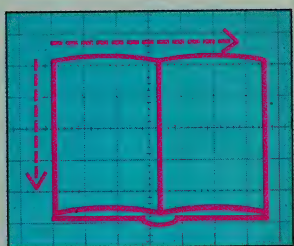

**LCD panel.** Gives clear indications of instrument settings, parameter values and selected control key functions at a glance, right next to the CRT screen.



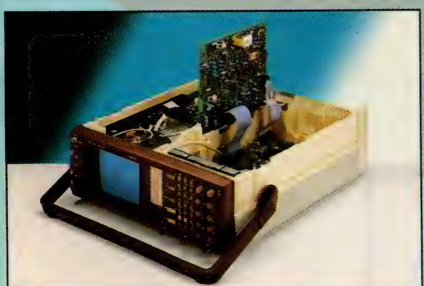

**Up/down controls.** Today's technology for fast, convenient input of amplitude (V/div.) and time (s/div.) settings. Fingertip operation – just press one way for up, and the other for down.




**Softkey function selection.** Multifunction softkeys simplify the front panel layout, and make operation clearer and more logical. An instantly accessible menu shows all available functions.



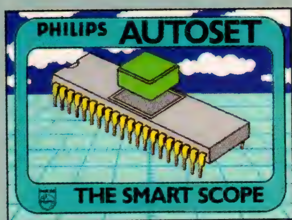
**All-new front-panel design.** The all-new front-panel design makes operation clearer and simpler. Control sequence is left to right, and top to bottom – just like reading a book!



**Designed for easy service.** PM 3050 was designed to make any required service fast and simple. Swing-up PCBs make access easy, and flat ribbon cables allow instant disconnection. Each oscilloscope has a complete, built-in testing routine, to provide a quick assurance of correct operation.

Unbeatable price!

Call your local Philips Organisation




*For full information about the PM 3050 scopes family, contact your local Philips sales organization or distributor, or: Philips I&E, HKF/55, 5600 MD Eindhoven, The Netherlands. Germany 0561-5010; UK 0223-358866; France 01-8301111; Italy 039-36351; Netherlands 040-782889; Sweden 08-7821000.*

## Philips PM 3050 family: setting the new standard

**CIRCLE NO 142**

DIGITAL
Over 1,000 components can be designed as a single data base.


## THE CAD WORKSTATION FOR EVERY PCB TECHNOLOGY.

Most CAD systems just can't handle today's complex PCB designs.

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We'll put you on the path to the future of PCB design.

**Telesis**

CIRCLE NO 169

# Monolithic Memories announces CMOS.

People tend to get a bit excited when they hear that Monolithic Memories is getting into CMOS.

And frankly, we can't blame them.

After all, we're doing things with CMOS that no one else has done before.

For instance, we're producing Double Density Interface and ZHAL™ circuits that run at CMOS power levels, with speeds rivalling the best of bipolar. And we're shipping them in volume.

We're also bringing CMOS to our PAL® product line, beginning with ZPAL™ devices


UPI/Bettmann


The ZL30 [ZL32] will give you the best of all worlds. A multi—functional, totally sophisticated tool designed with your needs firmly in mind **and already acknowledged as the "industry standard". Don't be fobbed off with pale imitations.**

Now you can have flexibility and speed in one high—speed production/ development system.

The ZL30 in conjunction with CUPL* software, plus a PC makes the most powerful workstation for PALs* and IFLs. In fact the **ZL30 is such a powerful combination that cloned lookalikes are inevitable. Don't be fobbed off with pale imitations.**

Remember, there's only one Stag and there's certainly only one ZL30.

■ Complete Stand—alone.
■ Will program most 20, 24 and 28 pin PAL*, EPLD and IFL.
■ Includes Altera 40 pin EPLD. ■ RS232C, IEEE—488 Interfaces, plus parallel handler interface. ■ Durable, function, Edit keyboard.
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*PAL — Monolithic Memories Inc.

**CIRCLE NO 160**

# NEWS BREAKS

EDITED BY JOAN MORROW

## 3-D GRAPHICS PROCESSOR PERFORMS 30M FLOPS

By implementing common graphics subroutines on semicustom ICs, the Graphicon 700 graphics processor from General Electric Co (Research Triangle Park, NC) manipulates 3-D images at a rate of 30M flops. The desk-side unit contains a 4M-byte display memory, which is expandable to 16M bytes, and drives a 1280×1024-pixel color display. It provides image-display options such as hidden-surface removal, wireframe representation, smooth and faceted shading, and multiple light sources.

It operates under control of a host computer over an Ethernet network or one of several parallel interfaces. More than 160 graphics-processing commands are available to Fortran or C programs running on the host. The $65,900 system (with monitor and interface) is the first product from the company's Silicon Systems Technology Department; this department will introduce other special-purpose processors, such as a data-retrieval system, later this year.—David Smith

## CMOS MAC CHIP MULTIPLIES 32-BIT NUMBERS IN 80 nSEC

The L64032 multiplier-accumulator (MAC) can multiply two 32-bit numbers in 80 nsec, even under worst-case commercial temperature and voltage conditions. The L64032, the first standard product from LSI Logic (Milpitas, CA), is an offshoot of the company's Macgen megacell compiler announced last month. The CMOS IC is as fast as announced bipolar MACs, but it consumes no more than 20% of the nominal current spec'd by the bipolar ICs. To facilitate system test, the chip incorporates scan testing that allows you to read and preload all on-chip registers. It's available in a 132-pin pin-grid array package for $350 (100). You can also use the L64032's layout as a basis for a custom-IC design.—David Smith

## SOFTWARE MODELS SIMULATE 64-BIT FLOATING-POINT PROCESSORS

Quadtree Software Corp (Bridgewater, NJ) is developing a behavioral-simulation software model of Weitek's (Sunnyvale, CA) 64-bit floating-point chip set, which comprises the WTL2264 and WTL2265. Weitek has agreed to certify the functional and timing accuracy of the software models before Quadtree releases them. The models are compatible with logic simulators from Mentor (Beaverton, OR), Daisy (Mountain View, CA), Silvar-Lisco (Menlo Park, CA), and HHB Systems (Mahwah, NJ). Quadtree anticipates that the models will be available in July for $1000 each.—Eva Freeman

## CAE WORKSTATION TOOLS EASE CUSTOM-IC AND PLD DESIGN

Two workstation products from Daisy Systems Corp (Mountain View, CA) support the layout of custom ICs and the design of programmable logic devices. First, the Cellmaster workstation provides the following facilities for the layout of cell-based custom ICs: an interactive floor planner (for planning chip layout), an automatic power-signal router, automatic placement and routing programs, a layout compactor, and correct-by-construction layout editors. The $125,000 workstation accepts cells directly from the company's Max mask editor; other sources of cells are also supported. The company is accepting orders now for delivery starting in July.

The second product allows you to create designs for PLDs using any combination of state-machine, schematic, and a textual high-level-language descriptions. The PLD Master software compiles designs using common PLD design tools including Abel, CUPL, and Amaze. It also simulates the designs and generates a JEDEC-format programming file for any PLDs supported by those tools. The $6500 software runs on any of the company's workstations.—David Smith

# NEWS BREAKS

### FAIRCHILD, HONEYWELL SIGN GATE-ARRAY SOURCING AGREEMENT

Fairchild Semiconductor Corp (Milpitas, CA) and Honeywell Inc (Colorado Springs, CO) have signed a bipolar-gate-array alternate-source agreement. The first two products to be covered by the agreement are Fairchild's FGE2500 and Honeywell's HE8000 gate arrays. The FGE2500 is a 2500-equivalent-gate ECL array, which uses a 1.5-$\mu$m bipolar technology. The HE8000 is an 8000-equivalent-gate device, which uses 1.25-$\mu$m CML/ECL bipolar technology.—Joan Morrow

### EPLDs OFFER 1800-GATE COMPLEXITY, 33-MHz OPERATION

Intel Corp (Folsom, CA) has introduced four erasable programmable logic devices (EPLDs) that can implement designs with complexities as large as 1800 equivalent 2-input gates and with clock frequencies as high as 33 MHz. The four devices include the 1800-gate 5C180, the 900-gate 5C090, the 300-gate 5C031, and an enhanced version of the 5C031 called the 5C032. The 300-gate devices can replace 20-pin bipolar PALs and offer as little as 100 $\mu$A of standby power consumption. Built with the company's CHMOS II-E EPROM process, these devices come in ceramic packages with windows (to allow you to erase and reprogram the devices) or lower-cost plastic DIPs. Prices start at $11.45 (100).

In a related announcement, Intel has added to its iPLDs PLD-design package an option that lets you build state-machine designs for implementation in the company's EPLDs. The iSTATE software supports syntaxes for state definition, for specification of state transitions, and for input and output signals. You can also include Boolean equations in your state-machine design. The $2500 iPLDs package runs on an IBM PC or compatible; an iSTATE upgrade to existing iPLDs installations costs $500.—David Smith

### LINEAR/DIGITAL SEMICUSTOM IC IMPLEMENTS CELL LIBRARY

The Flexible Linear Arrays (FLAs) from Exar Corp (Sunnyvale, CA) comprise three types of building blocks that can implement linear and digital functions in the vendor's soft-cell library. The blocks include a transistor block (the Twinstor) that you can configure as two npn common-collector transistors, two pnp common-base transistors, two matched resistors, or a 3-terminal pnpn switch. Similarly, the FLAs' Twinbooster block implements either a 500-mA npn or 50-mA pnp power transistor.

Circuits in the soft-cell library map directly onto the chips' blocks. For linear/digital IC designs, you can select op amps, comparators, bandgap references, Schmitt triggers, voltage-controlled oscillators and amplifiers, flip-flops, and multiplexers. Three FLAs are available: the B240 with 240 transistor blocks, the B180 with 180 transistor blocks, and the B100 with 99 transistor blocks. Turn-around time is six weeks min; NRE charges for layout and integration are $4800.—David Smith

### THIRD ANNUAL MICRO-BASED CADD FORUM TO BE HELD IN COLORADO

The Office of Research, Development, and Training at Colorado State University (Fort Collins, CO, (303) 491-5278) will hold its annual International Forum on micro-based CADD (computer-aided design/drafting) on September 17 through 19, 1986. The forum will focus on the major CADD software packages including Autocad, Cadkey, Cadvance, Cascade, P-CAD, Robocad, and Versacad. Forum seminar topics include a comparison between conventional and micro-based CADD, CADD networks, and artificial intelligence in CADD. Admission for the 3-day event is $295.—Steven H Leibson


Why fill your digital delay design with unnecessary components, when you can have all the capability you need in one small, low-cost IC?

TRW LSI Products Division, the industry leader in high performance digital signal processing products, gives designers an edge with the TDC1011. The TDC1011 is a high-speed, 8-bit wide shift register, programmable to any length between 3 and 18 stages. It operates at an 18MHz shift rate (56ns worst case), is TTL compatible, and dissipates a low 750mW.† The TDC1011 operates from a single +5V power supply and is available in a 24-lead DIP.

The beauty of the TDC1011 is that this single chip performs the same functions that would require as many as 18 alternative chips — instead of 18 shift registers, you can use just one in a variety of digital delay applications. This translates into lower component costs, less board space and reduced power dissipation. Built with TRW's OMICRON-B™ one-micron bipolar process, the TDC1011 provides the system designer with a unique variable delay capability at video speed.

You can use the TDC1011 for telecom, sonar, radar, CAT scanners, computer graphics, TV special effects, and a host of other digital delay applications. And, as with all of our products, the TDC1011 is backed by our extensive network of in-house and field applications engineers, application notes and our full line VLSI DATA BOOK.

Available off the shelf from Arrow Electronics, Hall-Mark and Hamilton/Avnet.

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# NEWS BREAKS: INTERNATIONAL

BY PETER HAROLD

## EUROPEAN VENDOR ENTERS MULTIBUS II COMPUTER BOARD MARKET

OSM Series Multibus II boards from Siemens (Munich, West Germany, TLX 5210025) include CPU, memory, and serial-interface cards. The CPU boards include the 80186-based OSM-B16, priced at DM 5500, and the 80286-based OSM-B26, priced at DM 7300. (An 80386 board is planned.)

The OSM-B16 accommodates as much as 512k bytes of onboard RAM; you can expand the OSM-B26's memory via its LBX II interface. The 32-bit OSM-B11X dual-ported memory boards offer capacities from 512k bytes to 4M bytes; they feature an 8k-byte cache that provides zero-wait-state cache-hit access via the LBX II bus. A 1M-byte memory board costs DM 7300. Additional boards include a RAM/ROM board, Ethernet and serial-communications boards, and a central-services module, which supports an interface to the company's Eurocard-based AMS-M Bus.

## MULTIMETERS FEATURE HIGH-RESOLUTION ANALOG, DIGITAL READOUTS

The M2000 line of handheld and portable multimeters from BBC Mettrawatt/Goerz (Nuremburg, West Germany, TLX 623729, or Wien, Austria, TLX 133161) feature digital- and analog-readout LCDs. Five 4-digit handheld models range from a simple autoranging model with a basic dc voltage accuracy of 0.7% to a manual/autoranging version with 0.1% dc-voltage accuracy. The 5-digit folding-case portable models have a basic dc voltage accuracy of 0.05% and feature a zoom facility that allows you to expand their analog-readout scale to an effective length in excess of 10m, yielding a resolution as high as one part in 7500. Additional features on selected versions include autoranging, peak-value hold, current-reading hold, relative measurement, decibel measurement, true rms measurement, and audible limit alarms. Prices range from $150 to $700.

## DEVELOPMENT SYSTEM SUPPORTS FORTH PROGRAMMING LANGUAGE

The Martello development system from British Telecom Microprocessor Systems (Ipswich, UK, TLX 98376) allows you to develop application software for STE Bus systems using the Forth programming language. The £1975 development system is based on a 10-slot STE Bus backplane; two 1M-byte, 3½-in. disk drives; and a CPU card with a ROM-based Forth-83 nucleus, interrupt handler, multitasking kernel, and disk filing system. The initial CPU offering is an 8085 $\mu$P. Support for other CPUs, together with approriate Forth nuclei, are planned. Disk-based program-development software includes a screen editor, macroassembler, debugger, floating-point package, ROM-code generator, and EPROM programmer.

## DATA-COMMUNICATIONS ANALYZER SUITS ISDN TESTING

The 2871 data-communications analyzer from Marconi Instruments (St Albans, UK, TLX 23350) performs in-service or out-of-service testing on data networks operating between 50 and 150k bps. For in-service testing, the £5500 analyzer monitors the framing bits of structured data traffic to estimate bit-error ratio. For out-of-service checks, the analyzer's pattern generator and error detector operate on a looped-back line and allow the instrument to monitor errors for as long as 30 hours. You can display a histogram of data-error timing on the instrument's integral CRT, or you can print out details of each error, together with its time of occurrence, on a printer. Data-line interfaces supported include RS-232C, RS-449, V35, and X21.

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**Get Results First Time, Everytime.** Don't miss important data because of set-up error. Nicolet scopes are easy to use. Find out how they can be the quickest solution to your signal problems. For more information, write Nicolet Oscilloscope Division, 5225 Verona Road, Madison, WI 53711. Or call 608/273-5008.

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For more information circle 1

# formers

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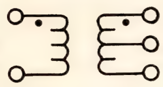
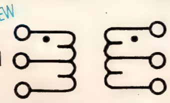
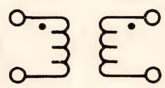
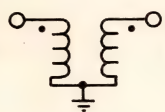
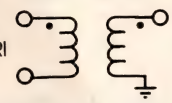
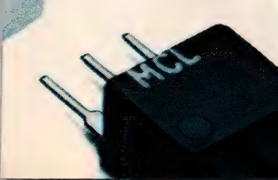
| case style number see opposite page. | | MODEL NO. | Ω RATIO | FREQUENCY MHz | INSERTION LOSS 3dB MHz | 2dB MHz | 1dB MHz | PRICE $ Ea. | Qty. |
|---|---|---|---|---|---|---|---|---|---|
| A*  PRI SEC | T | T1-1T | 1 | .05-200 | .05-200 | .08-150 | .2-80 | 3.95 | (10-49) |
| | | T1-6T NEW | 1 | .003-300 | .003-300 | .01-150 | .02-50 | 5.95 | (10-49) |
| | | T2-1T | 2 | .07-200 | .07-200 | .1-100 | .5-50 | 4.25 | (10-49) |
| | | T2.5-6T | 2.5 | .01-100 | .01-100 | .02-50 | .05-20 | 4.25 | (10-49) |
| | | T3-1T | 3 | .05-250 | .05-250 | .1-200 | .5-70 | 3.95 | (10-49) |
| | | T4-1 | 4 | .2-350 | .2-350 | .35-300 | 2-100 | 2.95 | (10-49) |
| | | T4-6T | 4 | .02-250 | .02-250 | .05-150 | 0.1-100 | 3.95 | (10-49) |
| | | T5-1T | 5 | .3-300 | .3-300 | .6-200 | .5-100 | 4.25 | (10-49) |
| | | T8-1T | 8 | .03-140 | .03-140 | .10-90 | 1-60 | 6.95 | (10-49) |
| | | T13-1T | 13 | .3-120 | .3-120 | .7-80 | 5-20 | 4.25 | (10-49) |
| | | T16-6T NEW | 16 | .03-75 | .03-75 | .06-30 | .1-20 | 4.95 | (10-49) |
| | TH | T4-1H | 4 | 8-350 | 8-350 | 15-300 | 25-200 | 4.95 | (10-49) |
| | TMO | TMO1-1T | 1 | .05-200 | .05-200 | .08-150 | .2-80 | 6.45 | (10-49) |
| | | TMO2-1T | 2 | .07-200 | .07-200 | .1-100 | .5-50 | 6.75 | (10-49) |
| | | † TMO2.5-6T | 2.5 | .01-100 | .01-100 | .02-50 | .05-20 | 6.75 | (10-49) |
| | | † TMO3-1T | 3 | .05-250 | .05-250 | .1-200 | .5-70 | 6.45 | (10-49) |
| | | TMO4-1 | 4 | .2-350 | .2-350 | .35-300 | 2-100 | 4.95 | (10-49) |
| | | TMO5-1T | 5 | .3-300 | .3-300 | .6-200 | 5-100 | 6.75 | (10-49) |
| | | TMO13-1T | 13 | .3-120 | .3-120 | .7-80 | 5-20 | 6.75 | (10-49) |
| B* NEW  PRI SEC | TT | TT1-6 | 1 | .004-500 | .004-500 | .02-200 | .1-50 | 5.95 | (10-49) |
| | | TT1.5-1 | 1.5 | .075-500 | .075-500 | .2-100 | .1-50 | 4.95 | (10-49) |
| | | TT2.5-6 | 2.5 | .01-50 | .01-50 | .025-25 | .05-10 | 5.25 | (10-49) |
| | | TT4-1 | 4 | .05-200 | .05-200 | .02-50 | 1-30 | 4.95 | (10-49) |
| | | TT25-1 | 25 | .02-30 | .02-30 | .05-20 | .1-10 | 7.95 | (10-49) |
| | TTMO | TTMO1-1 | 1 | .005-100 | .005-100 | .01-75 | .05-40 | 10.95 | (10-49) |
| C  PRI SEC | T | T1-1 | 1 | .15-400 | .15-400 | .35-200 | 2-50 | 2.95 | (10-49) |
| | | T1-6 NEW | 1 | .01-150 | .01-150 | .02-100 | .05-50 | 4.95 | (10-49) |
| | | T1.5-1 | 1.5 | .1-300 | .1-300 | .2-150 | .5-80 | 3.95 | (10-49) |
| | | T1.5-6 NEW | 1.5 | .02-100 | .02-100 | .05-50 | 0.1-25 | 4.95 | (10-49) |
| | | T2.5-6 | 2.5 | .01-100 | .01-100 | .02-50 | .05-20 | 3.95 | (10-49) |
| | | T4-6 | 4 | .02-200 | .02-200 | .05-150 | .1-100 | 3.95 | (10-49) |
| | | T9-1 | 9 | .15-200 | .15-200 | .3-150 | 2-40 | 3.45 | (10-49) |
| | | T16-1 | 16 | .3-120 | .3-120 | .7-80 | .5-20 | 3.95 | (10-49) |
| | | T36-1 | 36 | .03-20 | .03-20 | .05-10 | .1-5 | 5.95 | (10-49) |
| | TH | T1-1H | 1 | 8-300 | 8-300 | 10-200 | 25-100 | 4.95 | (10-49) |
| | | T9-1H | 9 | 2-90 | 2-90 | 3-75 | 6-50 | 5.45 | (10-49) |
| | | T16-1H | 16 | 7-85 | 7-85 | 10-65 | 15-40 | 5.95 | (10-49) |
| | TMO | TMO1-1 | 1 | .15-400 | .15-400 | .35-200 | 2-50 | 4.95 | (10-49) |
| | | TMO1.5-1 | 1.5 | .1-300 | .1-300 | .2-150 | .5-80 | 6.75 | (10-49) |
| | | † TMO2.5-6 | 2.5 | .01-100 | .01-100 | .02-50 | .05.20 | 6.45 | (10-49) |
| | | † TMO4-6 | 4 | .02-200 | .02-200 | .05-150 | .1-100 | 6.45 | (10-49) |
| | | TMO6-1 | 6 | .3-200 | .3-200 | .5-150 | 5-50 | 6.45 | (10-49) |
| | | TMO9-1 | 9 | .15-200 | .15-200 | .3-150 | 2-40 | 6.45 | (10-49) |
| | | TMO1.6-1 | 16 | .3-120 | .3-120 | .7-80 | 5-20 | 6.45 | (10-49) |
| D  PRI SEC | T | T2-1 | 2 | .025-600 | .025-600 | .05-400 | .5-200 | 3.45 | (10-49) |
| | | T3-1 | 3 | .5-800 | .5-800 | .2-400 | — | 4.25 | (10-49) |
| | | T4-2 | 4 | .2-600 | .2-600 | .5-500 | .2-250 | 3.45 | (10-49) |
| | | T8-1 | 8 | .15-250 | .15-250 | 25-200 | 2-100 | 3.45 | (10-49) |
| | | T14-1 | 14 | .2-150 | .2-150 | .5-100 | 2-50 | 4.25 | (10-49) |
| | TMO | TMO2-1 | 2 | .025-600 | .025-600 | .05-400 | .5-200 | 5.95 | (10-49) |
| | | TMO3-1 | 3 | .5-800 | .5-800 | 2-400 | — | 6.95 | (10-49) |
| | | TMO4-2 | 4 | .2-600 | .2-600 | .5-500 | 2-250 | 5.95 | (10-49) |
| | | TMO8-1 | 8 | .15-250 | .15-250 | .25-200 | 2-100 | 5.95 | (10-49) |
| | | TMO14-1 | 14 | .2-150 | .2-150 | .5-100 | 2-50 | 6.75 | (10-49) |
| E  PRI SEC | FT | FT1.5-1 | 1.5 | .1-400 | .1-400 | .5-200 | 1-100 | 29.95 | (1-4) |
| | FTB | FTB1-1 | 1 | .2-500 | .2-500 | .5-300 | 10-100 | 29.95 | (1-4) |
| | | FTB1-6 | 1 | .01-125 | .01-125 | .05-50 | .1-25 | 29.95 | (1-4) |
| | | ■ FTB1-1-75 | 1 | .5-500 | .5-500 | 5-300 | 10-100 | 29.95 | (1-4) |

■ Denotes 75 ohm models

* Maximum Amplitude Unbalance
0.1 dB over 1 dB frequency range
0.5 dB over entire frequency range

* Maximum Phase Unbalance
1.0° over 1 dB frequency range
5.0° over entire frequency range



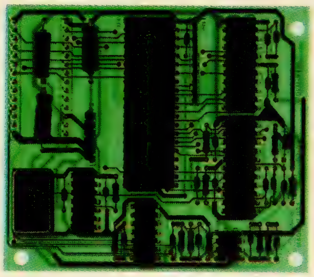

**CIRCLE NO 147**

C72-2 Rev. A

# When you positively custom

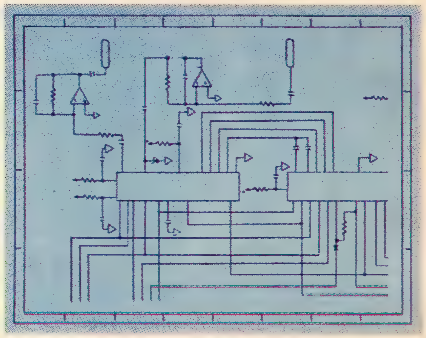
## Reliability

is your obvious first requirement in this vital link between your product and the outside world. At Ven-Tel —with 12 years experience and millions of modems designed and shipped—we don't take reliability for granted...*so you can.*



## Compatibility

with industry standards. All Ven-Tel modems utilize the industry standard "AT" command set, guaranteeing compatibility with virtually all types of software. And every Ven-Tel custom modem is fully compatible with our complete line of standard desktop and PC internal modems. We also meet Bell 212A and CCITT V.22bis standards in speeds up to 2400 baud.



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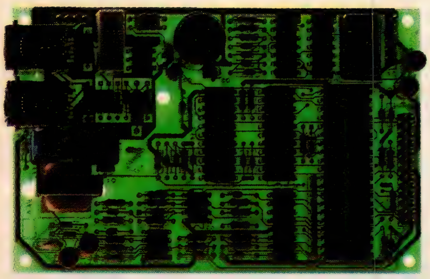
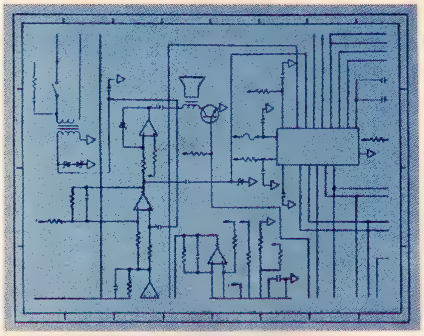
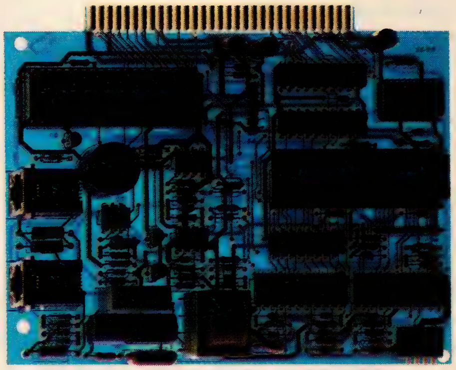
is more than a phrase to us. We've built a reputation for meeting product deadlines among some of the nation's largest and most demanding manufacturers. From start to finish in as little as 90 days, Ven-Tel can help you get your product to market quickly. You can even begin development using our standard modules while your design is being finalized.

# take a good

# absolutely, need reliable modems...







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your modem is your choice. From our standard off-the-shelf boards, to complete custom design, to licensing our proprietary CMOS chip design (for quantities in excess of 100,000 annually), we guarantee the right modem solution based on your deadline, design and volume requirements. Custom hardware configurations and firmware give you maximum freedom for integrating the modem into your overall product design.

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is an important requirement in applications like credit check terminals, portable computers and trouble monitors. Ven-Tel modem density is state-of-the-art to provide excellent "real estate" value, with complete auto-dial/auto-answer, AT compatible, 212A modems— in as little as 12 square inches. With power requirements as low as 500mW.

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2342 Walsh Avenue,
Santa Clara, CA 95051.

# look at Ven-Tel

CIRCLE NO 174

# SIGNALS & NOISE

### OTP ROMs are less expensive than UV EPROMs

Dear Editor:

The article "Enhanced 1-chip μCs" (EDN, January 9, pg 90) is a reasonably thorough introduction for the microcomputer novice. However, there are some points that need clarification. First, regarding E-PROMs, I think the article should have mentioned the cost difference between UV EPROMs and OTP ROMs. The same die is used for both, but the less expensive plastic package of the OTP ROM realizes a 20% cost reduction over the ceramic package/quartz window UV EPROM. (By the way, OTP ROMs and UV EPROMs can be erased by X-rays. Don't carry them through airport security.)

Second, although EEPROMs don't require special programming voltages, the addresses, data, and control signals must be applied to the chip during programming (as with UV EPROMs) and during erasure. If a PROM programmer isn't used, you must add programming circuitry to your microcomputer-based system. Adding this circuitry can be very costly, so it's impractical for program memory. The primary use of EEPROMs is for storing data to be updated infrequently or to be saved during power failure without the need for battery backup.

Finally, all microcomputers (not just "some") must have a way to read ROM so that the manufacturer can verify code at production time. Often this information is not public knowledge; nevertheless, it exists.

*Sincerely yours,*
*Jean C Campbell*
*Applications Engineering Manager*
*Single-chip microcomputers*
*NEC Electronics Inc*
*Natick, MA*

### Oops

In the March 6 issue of EDN, a portion of the VME Bus analog-I/O board tables (pgs 198 to 201) was misaligned because of an editing error. Further, Datel provided some information about its products that was unavailable at press time for the March 6 issue. A corrected version of this section of the tables appears on pg 32. In addition, there should be no entries in the analog-input columns for the Burr-Brown MPV905. We regret any confusion the error may have caused.

**WRITE IN**

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

## VME BUS ANALOG I/O BOARDS

| | | | ANALOG INPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|
| **MANUFACTURER** | **MODEL NUMBER** | **EUROCARD SIZE** | **CHANNELS** (SE/DIF) | **BEST RESOLUTION** (BITS) | **BEST ACCURACY** (% FSR) | **INPUT RANGES** (V) | **RANGING** | |
| **DATA SUD SYSTEMS** | DSSE16AD12-1 | D | 16/8 | 12 | — | 5, 10, ±5, ±10, 0 TO 20 mA, 4 TO 20 mA | LP | |
| | DSSE16AD12-2 | D | 16/8 | 12 | — | 5, 10, ±5, ±10, 0 TO 20 mA, 4 TO 20 mA, SPGA (x1 TO x1024) | LP/SP | |
| | DSSE8DA12 | D | | | | | | |
| **DATA TRANSLATION** | DT1402-F | D | 32/16 | 12 | 0.03 | 10, ±10, SPGA (x1, x2, x4, x8) | LP/SP | |
| | DT1414 | S | 16 SE | 12 + SIGN | 0.035 | ±5 | | |
| | DT1401 | D | 32/16 | 12 | 0.03 | 10, ±10, SPGA (x1, x2, x4, x8) | LP/SP | |
| | DT1401/5716 | D | 16 DIF | 16 | 0.0075 | ±10, SPGA (x1, x2, x4, x8) | SP | |
| | DT1405 | D | 32/16 | 12 | 0.01 | 10, ±10, SPGA (x1, x10, x100, x500) | LP/SP | |
| | DT1405/5716 | D | 16 DIF | 16 | 0.0075 | ±10, SPGA (x1, x10, x100, x500) | SP | |
| | DT1408 | D | 4 SE | 12 | 0.04 | 10, ±10 | LP | |
| | DT1403-2 | D | | | | | | |
| | DT1403-4 | D | | | | | | |
| | DT1406-8V | D | | | | | | |
| | DT1406-8M | D | | | | | | |
| | DT1406-8CL | D | 4 | — | — | TC, RTD, AND HI-LEVEL/4- TO 20-mA VERSIONS | — | |
| **DATEL** | DVME-602T, H | D | 4 DIF | 13 | 0.03 | TC, RTD, ±100 mV, ±5, 4 to 20 mA | LP/SP | |
| | DVME-611A, B | D | 32/16 TO 256 | 12 | 0.025 | ±5, ±10, 0 to 5, 0 TO 10, SPGA (x1, x2, x4, x8, x16, x32, x64, x128) | LP/SP | |
| | DVME-611C | D | 32/16 TO 256 | 14 | 0.01 | ±5, ±10, SPGA (x1, x2, x4, x8, x16, x32, x64, x128) | LP/SP | |
| | DVME-611D | D | 32/16 TO 256 | 16 | 0.0063 | ±5, ±10, SPGA (x1, x2, x4, x8, x16, x32, x64, x128) | LP/SP | |

| | | ANALOG OUTPUTS | | | | | | |
|---|---|---|---|---|---|---|---|---|
| CONVERSION TIME* (μSEC)** | MAXIMUM THROUGHPUT* (kHz)** | CHANNELS | RESOLUTION (BITS) | BEST ACCURACY (% FSR) | OUTPUT RANGES (V)** | SETTLING TIME (μSEC)** | PRICE | COMMENTS |
| 25 (TYP) | — | | | | | | — | A/D ISOLATION |
| 25 (TYP) | — | | | | | | — | A/D ISOLATION |
| | | 8 | 12 | — | 5, 10, ±5, ±10, 0 TO 20 mA, 4 TO 20 mA | 3 | — | |
| 4 | 125 | | | | | | $1945 | 16-LINE DIGITAL I/O; PACER CLOCK (1.66-μSEC TO 200-SEC INTERVAL) |
| 200 | — | | | | | | $395 | |
| 10 | 50 | 2 | 12 | 0.025 | 5, 10, ±5, ±10 | 20 MAX | $1595 | 16-LINE DIGITAL I/O; PACER CLOCK (1.66-μSEC TO 200-SEC INTERVAL) |
| 50 | 2.5 | 2 | 12 | 0.025 | 5, 10, ±5, ±10 | 20 MAX | — | 16-LINE DIGITAL I/O; PACER CLOCK (1.66-μSEC TO 200-SEC INTERVAL) |
| 10 | 50 | 2 | 12 | 0.025 | 5, 10, ±5, ±10 | 20 MAX | $1695 | 16-LINE DIGITAL I/O; PACER CLOCK (1.66-μSEC TO 200-SEC INTERVAL) |
| 50 | 2.5 | 2 | 12 | 0.025 | 5, 10, ±5, ±10 | 20 MAX | — | 16-LINE DIGITAL I/O; PACER CLOCK (1.66-μSEC TO 200-SEC INTERVAL) |
| 4 | 100 | 2 | 12 | 0.025 | 5, 10, ±5, ±10 | 20 MAX | $2095 | 16-LINE DIGITAL I/O; PACER CLOCK (1.66-μSEC TO 200-SEC INTERVAL) |
| | | 2 | 16 | 0.003 | ±10 | 10 | — | DEGLITCHED OUTPUTS |
| | | 4 | 16 | 0.003 | ±10 | 10 | — | DEGLITCHED OUTPUTS |
| | | 8 | 12 | 0.025 | 10, ±10 | 8 | $1495 | EXTERNAL REFERENCE-VOLTAGE INPUT |
| | | 8 | 12 | 0.025 | 4 TO 20 mA | 35 | $1495 | |
| | | 8 | 12 | 0.025 | 4- TO 20-mA CURRENT LOOP | 35 | — | |
| 33.3 mSEC | 30 Hz | | | | | | $1375 (T) $1419 (H) | |
| 20 (A), 4 (B) | 16 | | | | | | $1495 (A) $1617 (B) | |
| 35 | 18.7 | | | | | | $1638 | |
| 400 mSEC | 2.5 Hz | | | | | | $1648 | |

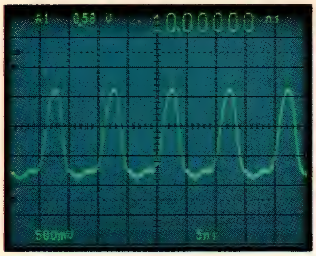
*Continued on pg 34*

## VME BUS ANALOG I/O BOARDS *(Continued)*

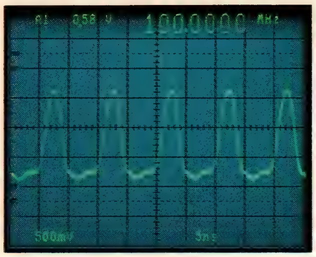
| | | | ANALOG INPUTS | | | | |
|---|---|---|---|---|---|---|---|
| MANUFACTURER | MODEL NUMBER | EUROCARD SIZE | CHANNELS (SE/DIF) | BEST RESOLUTION (BITS) | BEST ACCURACY (% FSR) | INPUT RANGES (V) | RANGING |
| DATEL | DVME-612A, B | D | 32/16 TO 256 | 12 | 0.025 | ±5, ±10, 0 TO 5, 0 TO 10, SPGA (x1, x2, x4, x8, x16, x32, x64, x128) | LP/SP |
| | DVME-612C | D | 32/16 TO 256 | 14 | 0.01 | ±5, ±10, SPGA (x1, x2, x4, x8, x16, x32, x64, x128) | LP/SP |
| | DVME-612D | D | 32/16 TO 256 | 16 | 0.0063 | ±5, ±10, SPGA (x1, x2, x4, x8, x16, x32, x64, x128) | LP/SP |
| | DVME-624V1, V2 | D | | | | | |
| | DVME-624C1, C2 | D | | | | | |
| | DVME-628V | D | | | | | |
| | DVME-628C | D | | | | | |

| CONVERSION TIME* (μSEC)** | MAXIMUM THROUGHPUT* (kHz)** | ANALOG OUTPUTS | | | | | PRICE | COMMENTS |
|---|---|---|---|---|---|---|---|---|
| | | CHANNELS | RESOLUTION (BITS) | BEST ACCURACY (% FSR) | OUTPUT RANGES (V)** | SETTLING TIME (μSEC)** | | |
| 20 (A), 4 (B) | 160 | 2 | 12 | 0.05 | ±5, ±10, 0 TO 5, 0 TO 10 | 10 | $1595 (A) $1712 (B) | |
| 35 | 18.7 | 2 | 12 | 0.05 | ±5, ±10, 0 TO 5, 0 TO 10 | 10 | $1732 | |
| 400 mSEC | 2.5 Hz | 2 | 12 | 0.05 | ±5, ±10, 0 TO 5, 0 TO 10 | 10 | $1742 | |
| | | 4 | 12 | 0.05 | ±2.5, ±5, ±10, 0 TO 5, 0 TO 10 | 30 (V1) 6 (V2) | $1446 (V1) $1360 (V2) | D/A ISOLATION |
| | | 4 | 12 | 0.05 | ±2.5, ±5, ±10, 0 TO 5, 0 TO 10, 4- TO 20-mA CURRENT LOOP | 30 (C1) 6 (C2) | $1363 (C1) $1577 (C2) | D/A ISOLATION |
| | | 8 | 12 | 0.05 | ±2.5, ±5, ±10, 0 TO 5, 0 TO 10 | 6 | $1345 | |
| | | 8 | 12 | 0.05 | ±2.5, ±5, ±10, 0 TO 5, 0 TO 10, 4- TO 20-mA CURRENT LOOP | 6 | $1708 | |

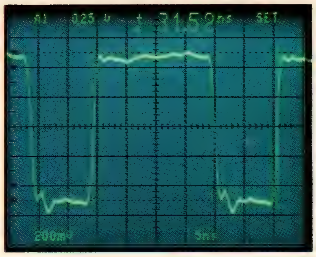
# SIXTEEN TOUGH ASSIGNMENTS.



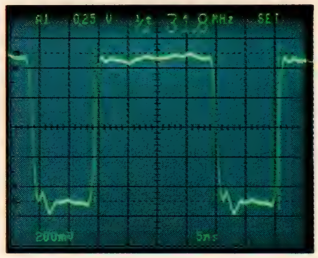
**A period measurement** is made on a 100 MHz clock using the extended accuracy and resolution of the Counter/Timer/Trigger in the 2465 DVS.



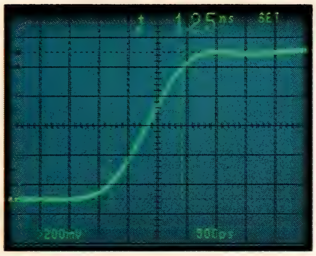
**A frequency measurement** is made with the same high precision. Simply press two buttons, and the period measurement on the left is converted to frequency.



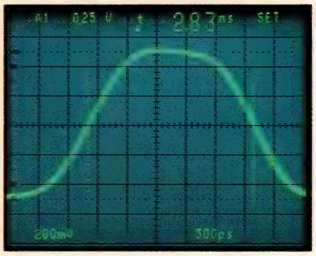
**Short time intervals** can be measured most accurately with the easy-to-use time cursors. They also make quick work of longer intervals, with 1% accuracy.



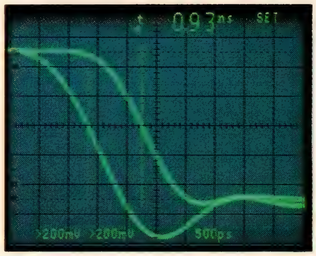
**Calculated frequency** takes only seconds. The time cursor measurement on the left can be converted to frequency with push-button ease and 1% accuracy.



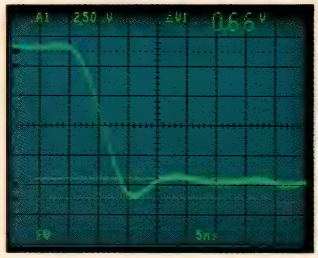
**This fast-pulse rise time** is nearly that of the scope. The 2465 achieves maximum bandwidth with minimum waveform aberrations. This level of pulse



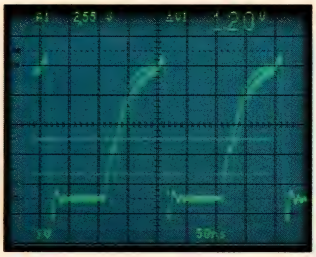
response ensures that **pulse width** and amplitude measurements on fast waveforms (above) truly reflect conditions in a circuit under test.



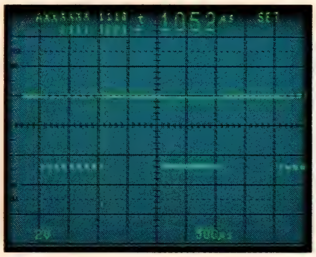
**Propagation delay** measurement accuracy is assured by built-in propagation delay matching. Delay between Channels 1 and 2 can be corrected to the probe tip.



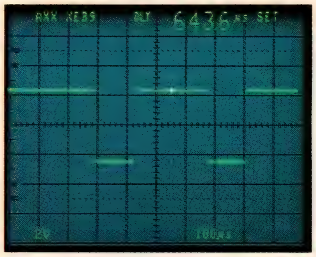
**Overshoot and ringing** measurement accuracy requires flat response in a probe/oscilloscope system. Tek probes and scopes are designed to work together.



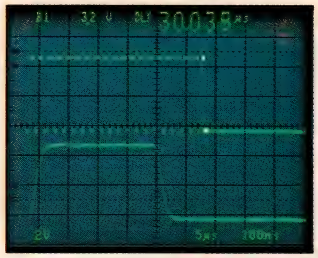
**Logic-level violations** can be spotted quickly on a TTL waveform (above) with measurement cursors set to define logic-level boundaries.



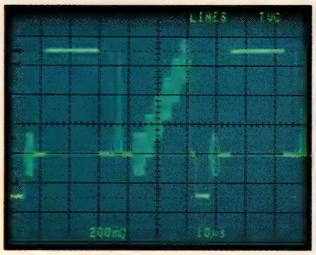
**The Word Recognizer** (with a binary word) is used to pick out a pulse train in a data stream. The time cursors measure pulse train duration.



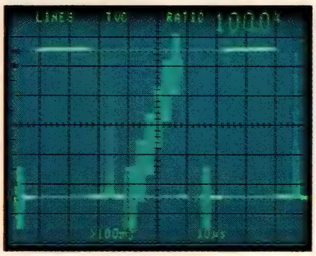
**Identify a word position.** The Word Recognizer (in HEX) is intensifying a word position and measuring delay relative to a waveform on another line.



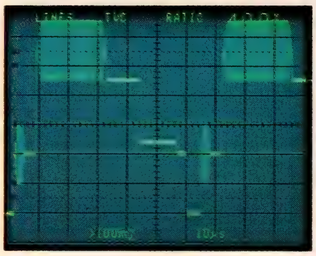
**Delayed sweep** is used to expand the last pulse in a pulse train. The intensified zone identifies the expanded pulse position.



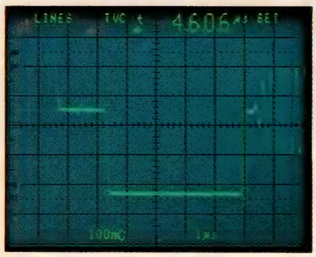
**TV line trigger** in the 2465 DVS displays a full-field composite test signal. The built-in TV clamp circuit removes hum and tilt on the ac-coupled video.



**Calibrate cursors** in IRE units with variable attenuation. Blanking level to reference white level is defined as 100 IRE units in NTSC video.



**Burst amplitude** should be 40 IRE units in NTSC video. The cursors quickly measure other waveform amplitudes. Field triggering checks any line.



**Sync width** and blanking are common, easy-to-make timing measurements. Accurate time measurements can be made anywhere in a video system.

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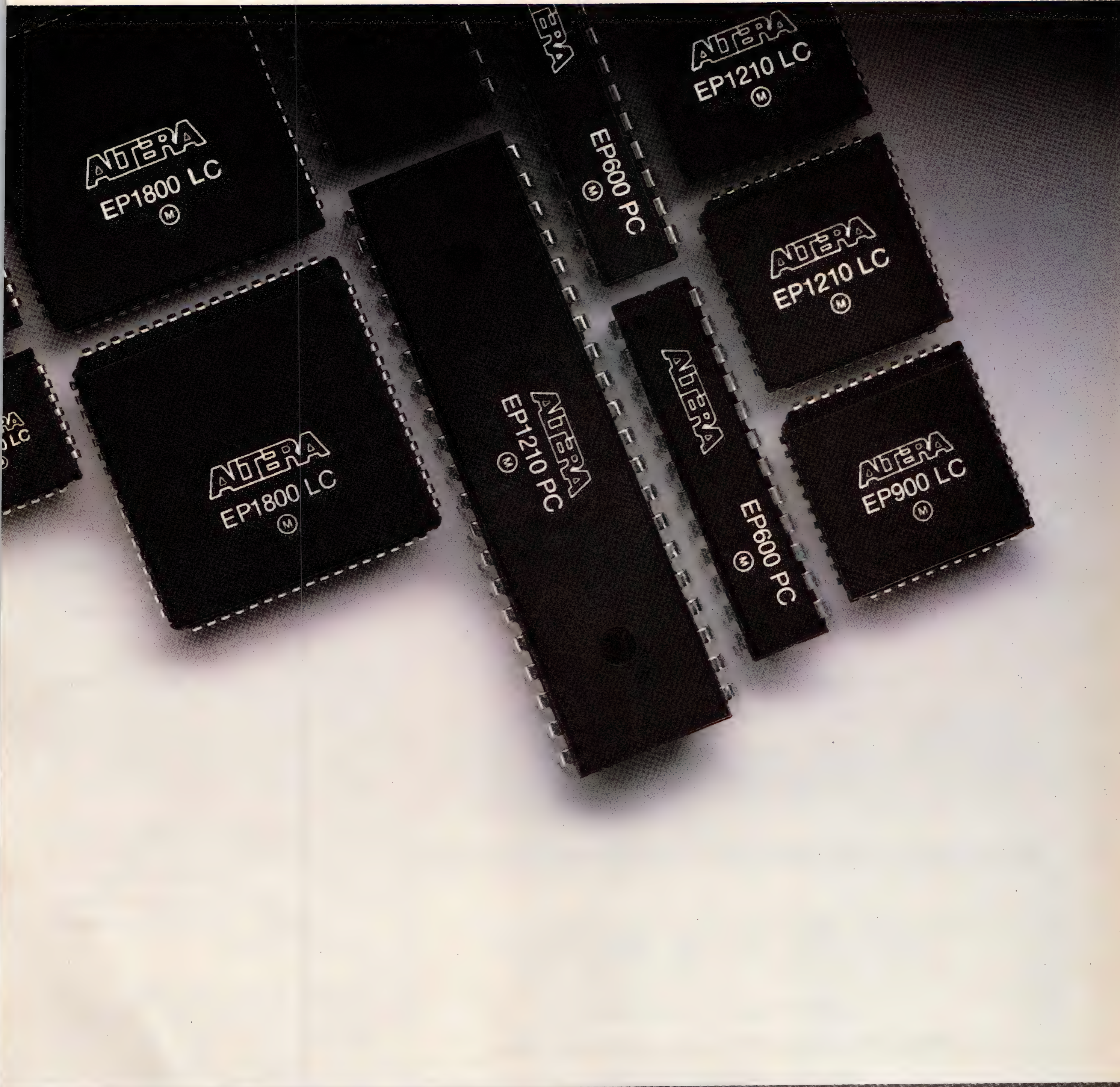
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EP1210 LC
EP600 PC
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EP1800 LC
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EP1210 PC
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EP900 LC

# CALENDAR

**International Communications Association (ICA) Annual Conference and Exposition,** Atlanta, GA. ICA, 12750 Merit Dr, Suite 710, LB-89, Dallas, TX 75251. (214) 233-3889. June 1 to 6.

**Surface-Mount Technology Design Workshop,** Toronto, CA. IPAC, Box 1869, Los Gatos, CA 95031. (408) 354-0700. June 2 to 3.

**Digital Signal Processing Fundamentals** (short course), Atlanta, GA. Department of Continuing Education, Georgia Institute of Technology, Atlanta, GA 30332. (404) 894-2402. June 2 to 4.

**III-V Semiconductor Materials and Devices** (short course), Palo Alto, CA. Continuing Education in Engineering, University of California Extension, 2223 Fulton St, Berkeley, CA 94720. (415) 642-4151. June 2 to 4.

**Power Spectrum Estimation** (short course), Atlanta, GA. Department of Continuing Education, Georgia Institute of Technology, Atlanta, GA 30332. (404) 894-2402. June 2 to 4.

**Vision '86** (Applied Machine Vision Conference and Exposition), Detroit, MI. Society of Manufacturing Engineers, Box 930, Dearborn, MI 48121. (313) 271-1500. June 2 to 5.

**68000 Microprocessor** (short course), Rochester, NY. College of Continuing Education, Rochester Institute of Technology, 60 W Main St, Rochester, NY 14614. (716) 475-2234. June 2 to 6.

**Circuit Expo '86 West,** Long Beach, CA. Worldwide Convention Management Co, Box 159, Libertyville, IL 60048. (312) 362-8711. June 3 to 5.

**Power Europa '86,** Wiesbaden, West Germany. TCM Expositions Ltd, Exchange House, 33 Station

# CALENDAR

Rd, Liphook, Hampshire, GU30 7DN, England. (0428) 724660. June 3 to 5.

**Defense Data Networking and DoD Protocol Standards** (short course), University of Maryland, College Park, MD. (301) 985-7157. June 4 to 6.

**Digital Speech Processing** (short course), Atlanta, GA. Department of Continuing Education, Georgia Institute of Technology, Atlanta, GA 30332. (404) 894-2402. June 4 to 6.

**International Conference on Consumer Electronics,** Rosemont, IL. Michael Ross, Conference Chairman, RCA David Sarnoff Research Center, Princeton, NJ 08540. (609) 734-2975. June 4 to 6.

**Local Area Networks** (short course), Atlanta, GA. Center for Advanced Professional Education, 1820 E Garry St, Suite 110, Santa Ana, CA 92705. (714) 261-0240. June 4 to 6.

**Multidimensional Digital Signal Processing** (short course), Atlanta, GA. Department of Continuing Education, Georgia Institute of Technology, Atlanta, GA 30332. (404) 894-2402. June 4 to 6.

**Network Management/Technical Control Conference and Exposition**, Boston, MA. CW/Conference Management Group, 375 Cochituate Rd, Framingham, MA 01701. (617) 879-0700. June 9 to 12.

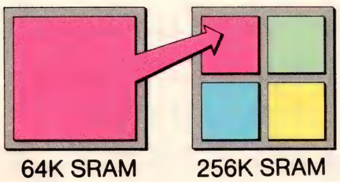
**Comdex/International,** Nice, France. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. June 10 to 12.

**Distributed Operating Systems** (short course), University of Maryland, College Park, MD. (301) 985-7157. June 10 to 12.

# 256K SRAM

# In Quantity Now!


NEC's 256 Kbit static RAM in advanced silicon-gate CMOS technology is hard to match on price/performance ratio. Working off a single 5V supply, the µPD43256C offers quadruple capacity with access times down to 100 ns. As little as 2V guarantees data retention. The high speed and low power consumption results from a unique new circuitry technique developed by NEC.




Better still, delivery times for quantity orders of the µPD43256C are down to the absolute minimum – with maximum quality maintained by NEC's tough product testing which combines double screening and a 100% burn-in.

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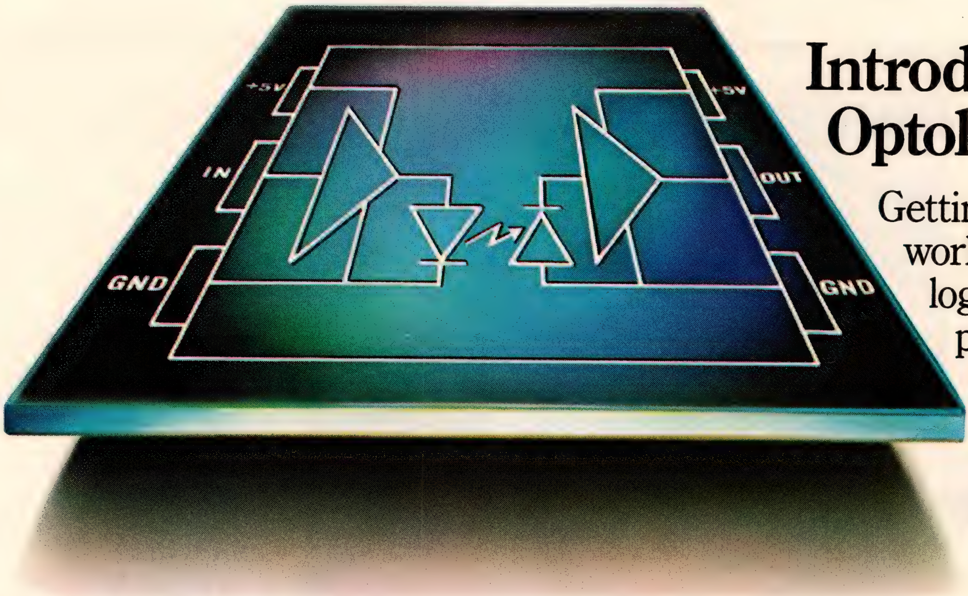
NEC

CIRCLE NO 57

# Our new Opto
# like a d




## Introducing the Optologic™ Coupler.

Getting lost in the analog world is no fun for the logic designer. In the past you had to consider trade-offs between input current, LED temperature dependence, speed and many other parameters. Many of these trade-offs were figured out by trial and error. It was really time consuming. And a real pain. But now there's good news ahead.

**A new concept.**

Now you can achieve optoisolator protection without having to understand the analog operation of the optocoupler.

The Optologic coupler is the first general purpose, high speed optoisolator that looks exactly like any common 74-series logic gate at both input and output. This makes it extremely easy to interface between same or different logic families. The innovative use of an input amplifier ensures real LSTTL compatibility and preserves your TTL noise immunity.

The Optologic coupler will find wide use in data communications. In local area networks you can greatly improve noise immunity while utilizing the device's high input impedance in multiple bridged line receivers.

---

**The Optologic coupler is available from these distributors:**

U.S.

ARROW ELECTRONICS, INC.
BELL INDUSTRIES
(GRAHAM DIVISION)
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HAMMOND ELECTRONICS, INC.
HARRISON EQUIP. CO., INC.
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# isolator thinks
# gital IC.

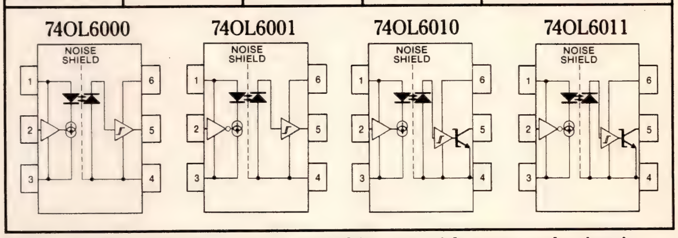
In another common application, AC/DC precision level sensing is possible because of the well-defined input threshold.

And the price is competitive with other high speed optocouplers.

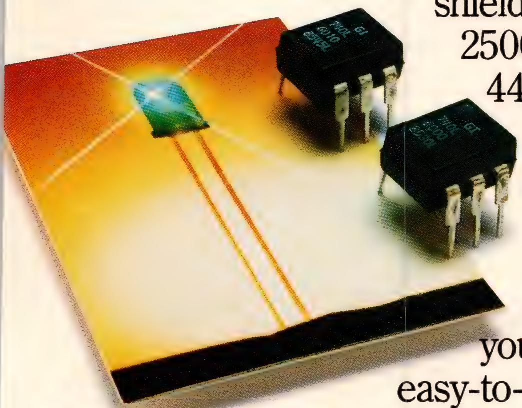
**High performance and reliability.**

Propagation delay of the Optologic coupler is 60ns and supports datacom to 15 MBaud. The built-in internal noise shield offers 15kV/$\mu$s common mode transient rejection.

| PART NUMBER | LOGIC COMPATIBILITY | | LOGIC FUNCTION | OUTPUT CONFIGURATION |
|---|---|---|---|---|
| | INPUT | OUTPUT | | |
| 74OL6000 | LSTTL | TTL | BUFFER | TOTEM POLE |
| 74OL6001 | LSTTL | TTL | INVERTER | TOTEM POLE |
| 74OL6010 | LSTTL | CMOS | BUFFER | OPEN COLLECTOR |
| 74OL6011 | LSTTL | CMOS | INVERTER | OPEN COLLECTOR |




There are two output versions available: one with totem pole circuit configuration for TTL compatibility, and another with open collector for interface to 4.5 V to 15 V CMOS or power transistors.



2500 VAC RMS isolation for one minute corresponds to a 440 VAC working voltage.

MTTF is 1.68 million hours at 90% confidence.

The Optologic coupler is a fool-proof device that provides a level of design integrity and security that the engineer has not had before.

If you hate leaving the digital world every time you want to optically isolate your circuits, design in the easy-to-use Optologic couplers from the LightHouse.

All you do is plug them in.

And bingo.

For samples or information about immediate volume production, contact your local distributor or General Instrument, Optoelectronics Division, 3400 Hillview Avenue, Palo Alto, CA 94304. (415) 493-0400. TWX: 470208.

**GENERAL INSTRUMENT**
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The LightHouse you can depend on.

CIRCLE NO 90

**CANADA**

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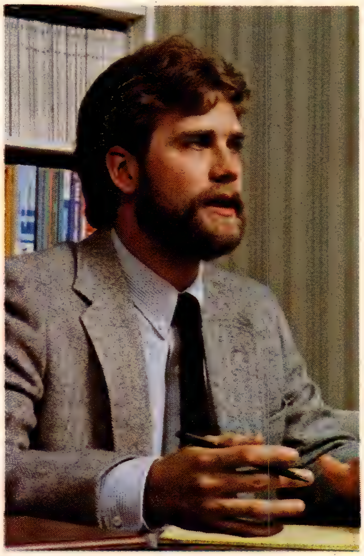
# Misapplication specific



In the rush to create memorable product names and catchy acronyms, electronics companies sometimes misuse and abuse the terminology that we depend on to clarify abstruse technical concepts. No term is more misused than "application specific," usually as used in application-specific integrated circuit, or ASIC. An ASIC used to be a chip whose function you, the user of the chip, would design. Some vendors now indiscriminately apply the term to memory chips, power devices, and almost any other type of chip. The term seems to apply to any product that serves some applications but not others—ie, all of them.

Consider one definition of an application-specific memory: an IC containing a memory core surrounded by logic functions that "make it suitable for a particular application." The same source of that obscure definition attempts to divide the application-specific category into customer application-specific ICs and application-dedicated ICs. What were once properly regarded as ASICs are now single-customer application-specific devices; furthermore, gate arrays that include some special features would be application-specific ASICs.

To set the record straight, application-specific ICs are full-custom ICs, standard-cell-based ICs, gate arrays, and programmable logic devices. Period. These devices are specific to a customer's application because the customer in some way designs the functional content of the chip.

To consider a memory chip application-specific just because it was designed for certain applications opens a Pandora's box. For example, surface-mounted devices could be application-specific; they are designed for applications requiring utmost packing density. You could also consider resistors with values greater than 1 MΩ to be application-specific; they suit applications requiring low power consumption or isolation. One vendor has even noted, "We've been in ASICs for 20 years. We just didn't call them ASICs. We called them power transistors."

Using an ASIC label for a vendor-designed, commodity IC misleads customers and dilutes the real benefit of those technologies that really are application-specific. This practice leads to confusion in an industry already swamped with information, and it adds nothing to a potential user's understanding of a product. It also establishes bizarre precedents. You could call this editorial misapplication-specific; it addresses the misapplication, to the point of meaninglessness, of the terms we need to communicate.

David Smith

**David Smith**
**Associate Editor**

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**CIRCLE NO 187**

# IN MEMORIES.

## We are the leader in 1Mb DRAMs. In 256K static RAMs, CMOS EPROMs and 1Mb ROMs. Yet, people still think of us only as the world leader in CMOS and NMOS static RAMs.

We are the world leader in CMOS and NMOS static RAMs, in 16K, 64K and 256K byte wide memory products. We make the fastest 2K x 8 at 35 ns and also a 4K x 4 static RAM at 35 ns. We pioneered the 8K x 8 CMOS static RAM and are now offering a 64K x 1 (55 ns) and 32K x 8 CMOS static RAM.

But we make more than static RAMs. As you can see from the chart, we have a complete line of DRAMs, CMOS, and NMOS ROMs, EPROMs, and one time programmables. And they are all in volume production today.

## Tradition of being first.

We were also the first to introduce the 1 Mb DRAM and we're now the market leader. We were one of the first suppliers of the 256K CMOS static RAM. We were a leader with the 256K ROM and within a year of introduction, we shipped more than all other suppliers combined. And we are matching that with our 1 Mb CMOS mask ROM.

So you can see that we have the capability to supply the memory products you want—when you want them.

That's memory power; that's Toshiba.

**TOSHIBA MEMORY PRODUCT SUMMARY**

| PART NO. | ORG. | PROCESS | SAMPLES | PROD. | SPEED SORTS AVAILABLE (ns) | | | | PACKAGE OPTIONS |
|---|---|---|---|---|---|---|---|---|---|
| **DYNAMIC RAMS** | | | | | | | | | |
| TMM4164AP | 64KX1 | NMOS | YES | YES | 150 | 200 | | | P |
| TMM41256P | 256KX1 | NMOS | YES | YES | 120 | 150 | | | PT |
| TMM41257P | 256KX1 | NMOS | YES | YES | 120 | 150 | | | PT |
| TMM41464P | 64KX4 | NMOS | YES | YES | 120 | 150 | | | P |
| TC511000C | 1MbX1 | CMOS | YES | YES | 100 | 120 | | | C |
| TC511000P/J | 1MbX1 | CMOS | YES | 2Q'86 | 100 | 120 | | | PJ |
| TC511001C | 1MbX1 | CMOS | YES | YES | 100 | 120 | | | C |
| TC511001P/J | 1MbX1 | CMOS | YES | 2Q'86 | 100 | 120 | | | PJ |
| TC511002P/J | 1MbX1 | CMOS | YES | 2Q'86 | 100 | 120 | | | PJ |
| TC514256P | 256KX4 | CMOS | YES | 2Q'86 | 100 | 120 | | | P |
| TC514257P | 256KX4 | CMOS | YES | 2Q'86 | 100 | 120 | | | P |
| **STATIC RAMS** | | | | | | | | | |
| TMM2114AP | 1KX4 | NMOS | YES | YES | 120 | 150 | | | P |
| TMM2016AP | 2KX8 | NMOS | YES | YES | 90 | 100 | 120 | 150 | P |
| TMM2016BP | 2KX8 | NMOS | YES | YES | 90 | 100 | 120 | 150 | P |
| TMM2015AP | 2KX8 | NMOS | YES | YES | 90 | 100 | 120 | 150 | P |
| TMM2015BP | 2KX8 | NMOS | YES | YES | 90 | 100 | 120 | 150 | P |
| TMM2064P | 8KX8 | NMOS | YES | YES | 100 | 120 | 150 | | P |
| TMM2063P | 8KX8 | NMOS | YES | YES | 100 | 120 | 150 | | P |
| TC5504AP | 4KX1 | CMOS | YES | YES | 200 | 300 | | | P |
| TC5514AP | 1KX4 | CMOS | YES | YES | 200 | 300 | | | P |
| TC5516/17AP | 2KX8 | CMOS | YES | YES | 200 | 250 | | | PFY |
| TC5517/18BP | 2KX8 | CMOS | YES | YES | 200 | 250 | | | PFY |
| TC5517/18CP | 2KX8 | CMOS | YES | YES | 150 | 200 | | | PFY |
| TC5565P | 8KX8 | *CMOS | YES | YES | 120 | 150 | | | PFY |
| TC5565AP | 8KX8 | *CMOS | 2Q'86 | 2Q'86 | 100 | 120 | | | PFY |
| TC5563AP | 8KX8 | *CMOS | 2Q'86 | 2Q'86 | 100 | 120 | | | PFY |
| TC5564P | 8KX8 | CMOS | YES | YES | 150 | 200 | | | PY |
| TC55257P | 32KX8 | *CMOS | YES | YES | 100 | 120 | 150 | | P |
| **HIGH SPEED STATIC RAMS** | | | | | | | | | |
| TMM2018D | 2KX8 | NMOS | YES | YES | 35 | 45 | 55 | | D |
| TMM2068D | 4KX4 | NMOS | YES | YES | 35 | 45 | 55 | | D |
| TMM2078D | 4KX4 | NMOS | YES | YES | 35 | 45 | 55 | | D |
| TC5561P | 64KX1 | *CMOS | YES | YES | 70 | | | | P |
| TC5562P | 64KX1 | *CMOS | YES | YES | 45 | 55 | | | P |
| **EPROMS** | | | | | | | | | |
| TMM2764D | 8KX8 | NMOS | YES | YES | 150 | 200 | 250 | | D |
| TMM2764DI | 8KX8 | NMOS | YES | YES | 150 | 200 | 250 | | D |
| TMM2764AD | 8KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TMM27128D | 16KX8 | NMOS | YES | YES | 150 | 200 | 250 | | D |
| TMM27128DI | 16KX8 | NMOS | YES | YES | 150 | 200 | 250 | | D |
| TMM27128AD | 16KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TMM27256D | 32KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TMM27256DI | 32KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TMM27256AD | 32KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TC57256D | 32KX8 | CMOS | YES | YES | | 200 | 250 | | D |
| TMM27512D | 64KX8 | NMOS | YES | YES | | 200 | 250 | | D |
| **ONE TIME PROGRAMMABLES** | | | | | | | | | |
| TMM2464AP | 8KX8 | NMOS | YES | YES | 200 | | | | PF |
| TMM24128AP | 16KX8 | NMOS | YES | YES | 200 | | | | PF |
| TMM24256AP | 32KX8 | NMOS | YES | YES | 200 | | | | PF |
| TMM24512P | 64KX8 | NMOS | 2Q'86 | 2Q'86 | 250 | | | | PF |
| **MASK ROMS** | | | | | | | | | |
| TC5364/5/6P | 8KX8 | CMOS | YES | YES | 250 | | | | P28 |
| TMM23256P | 32KX8 | NMOS | YES | YES | 150 | | | | P28 |
| TC53257P | 32KX8 | CMOS | YES | YES | 200 | | | | FP28 |
| TC53512P | 64KX8 | CMOS | YES | 2Q'86 | 200 | | | | P28 |
| TC531000P | 128KX8 | CMOS | YES | YES | 200 | | | | P28 |
| TC532000P | 256KX8 | CMOS | YES | 2Q'86 | 200 | | | | P32 |

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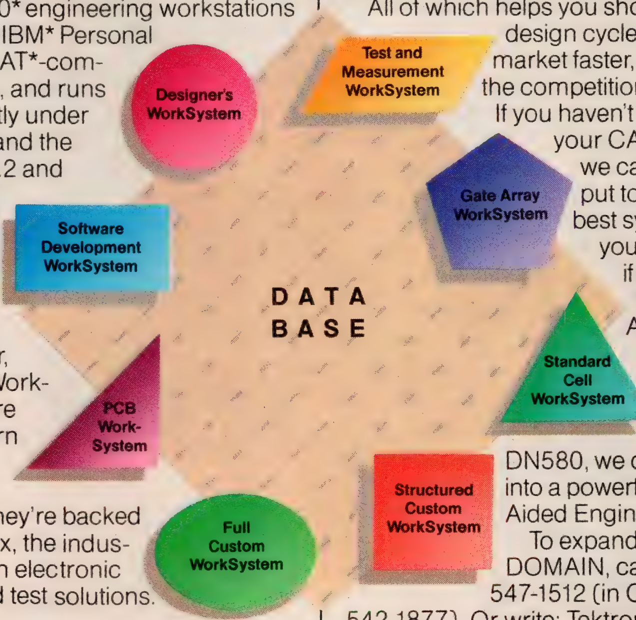


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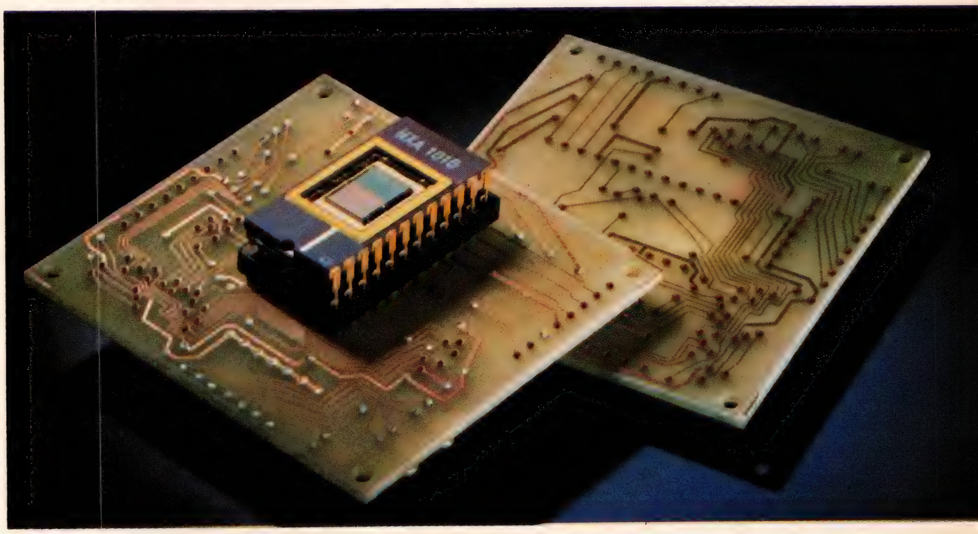
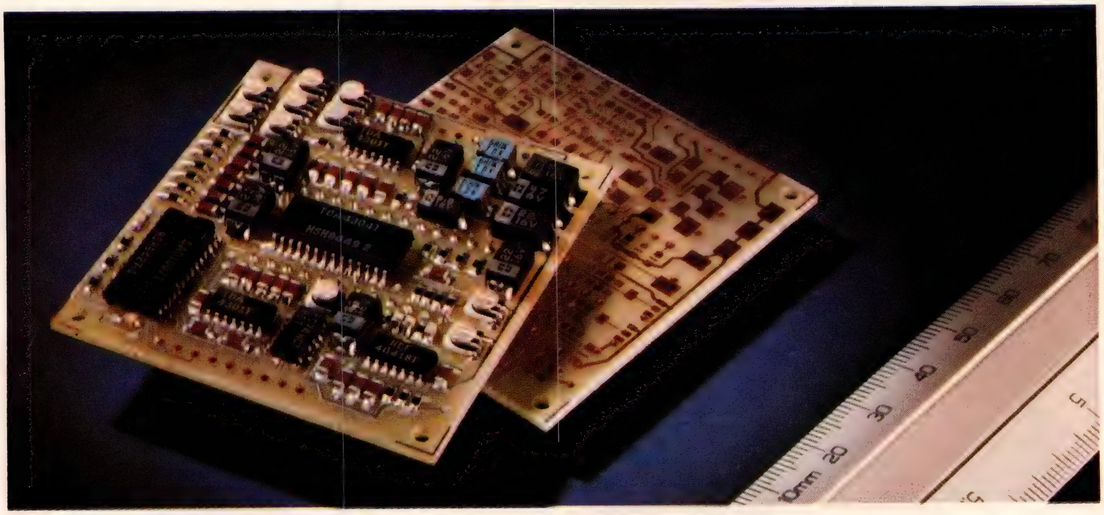
CIRCLE NO 171

# Solid-state area-scan image sensors vie for machine-vision applications

Peter Harold, *European Editor*

A solid-state area-scan image sensor requires that you add little more than a lens and a few ICs to create a computer system with vision capabilities. These sensors compare favorably with line-scan types and the familiar TV vidicon tubes, but because many low-cost, high-resolution area-scan image sensors are designed as direct replacements for those vidicon tubes, their scanning speeds are far from ideal for many industrial and scientific machine-vision systems. Choosing the right area-scan image sensor for your application may thus involve a tradeoff between a variety of factors: resolution, exposure control (scan speed), spectral response, interfacing requirements, and price.





***Following the standard format of a ½-in. camera tube,*** *the NXA1010 frame-transfer CCD image sensor from Philips* ***(top)*** *produces two CCIR-compatible, 294-line interlaced fields to achieve 604×576-pixel resolution. The control board* ***(bottom)*** *contains most of the scan-control logic required by the sensor, and it measures only 60 mm².*

In order to build a 2-D image of an object, line-scan sensors require mechanical scanning, either by moving the target object or by including optical components—such as a mirror—within the camera. Area-scan image sensors don't have this requirement, and they are therefore well suited to applications, such as robot vision systems, in which you can't control the motion of the target. In addition, their high degree of spatial stability and freedom from image-scanning nonlinearities recommends them to noncontact measurement applications. Solid-state area-scan image sensors are preferable to vidicon-tube sensors in industrial environments because they operate from low voltages, come in rugged DIPs, and survive for long periods without realignment.

To extract image information from their 2-D photosensitive arrays, however, area-scan devices must incorporate on-chip scanning logic, which limits your flexibility in controlling the image-scanning process. Most area-scan devices scan at slow, TV-standard speeds; the interlacing method produces a flicker that the human eye will forgive but an industrial computer won't. What's more, you usually can't vary the scanning procedure in order to focus on particular parts of an image. This limited control makes it difficult to adjust exposure times and to maintain the integrity of indi-

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**CIRCLE NO 149**

vidual pixel information. The degree to which you can manipulate exposure control depends on the type of area-scan image sensor you choose.

**Vidicon replacements**

Solid-state image sensors designed to replace tube-type sensors (typically vidicons) in CCTV, home video, and electronic-news-gathering (ENG) cameras currently are the largest growth segment in the market for area-scan devices. These devices provide high resolution—as high as 1280×980 pixels in NEC's latest offering—and a wide spectral response, from below 400 to approximately 1000 nm. In addition, because they're intended for consumer and industrial markets, which demand parts in large quantities, these image sensors are available at relatively low cost.

Although the resolutions achieved by vidicon-replacement-type image sensors may appear ideal for machine-vision systems, straightforward horizontal and vertical pixel counts don't tell the whole story. You must also consider the structure of the image-sensing array—ie, the relative placement on the silicon of the photosensitive pixels and the associated scanning circuitry. This structure determines the percentage of the imaging area that's actually sensitive to incident light.

All area-scan image sensors exhibit some degree of obscuration (ie, the proportion of the imaging area insensitive to light). Source points of light from the target that strike this insensitive area will remain totally undetected. The insensitive area is the cumulative distribution of surface area not covered by photosensitive pixels, an area usually consumed by the scanning circuitry. An ideal sensor would exhibit no surface obscuration; each source point of light from the target would be guaranteed to contribute to at least one pixel's output. The sensor must leave room for the scanning circuitry, however, so there will always be some insensitive regions of a sensor's surface area.

Two types of photosensitive element predominate in the manufacture of vidicon-replacement-type image sensors: charge coupled devices (CCDs) and photodiode arrays (the former are also used for the scanning logic in some devices). Sensor structure, however, inheres in the method of accessing the image information, rather than in the composition of the sensing element itself, and the degree of obscuration on the imaging surface depends on this method of information access.

The interline-transfer arrangement, the method used by NEC in its image sensors, consists of an array of photodiodes arranged in vertical columns; the scanning circuitry consists of light-shielded CCD analog shift registers placed vertically between each column of photodiodes (**Fig 1**). At the end of each frame period, the photon-induced charge accumulated by each photodiode is transferred to the vertical CCD shift registers for storage. During the next frame period, the pixel information from the previous frame is shifted down into a horizontal CCD shift register to provide an output equivalent to a normal TV picture scan.

Although this arrangement can lead to as much as 50% obscuration on the horizontal axis, it does achieve efficient silicon usage—ie, it produces a high resolution on a minimum die size—and so contributes to higher yields and lower part costs. Using this arrangement, NEC's area-scan image sensors provide a horizontal resolution of 1280 pixels, a vertical resolution of 980 pixels, and a total imaging area equivalent to a 1-in. vidicon tube.

Philips's and English Electric Valve's frame-transfer sensors use a

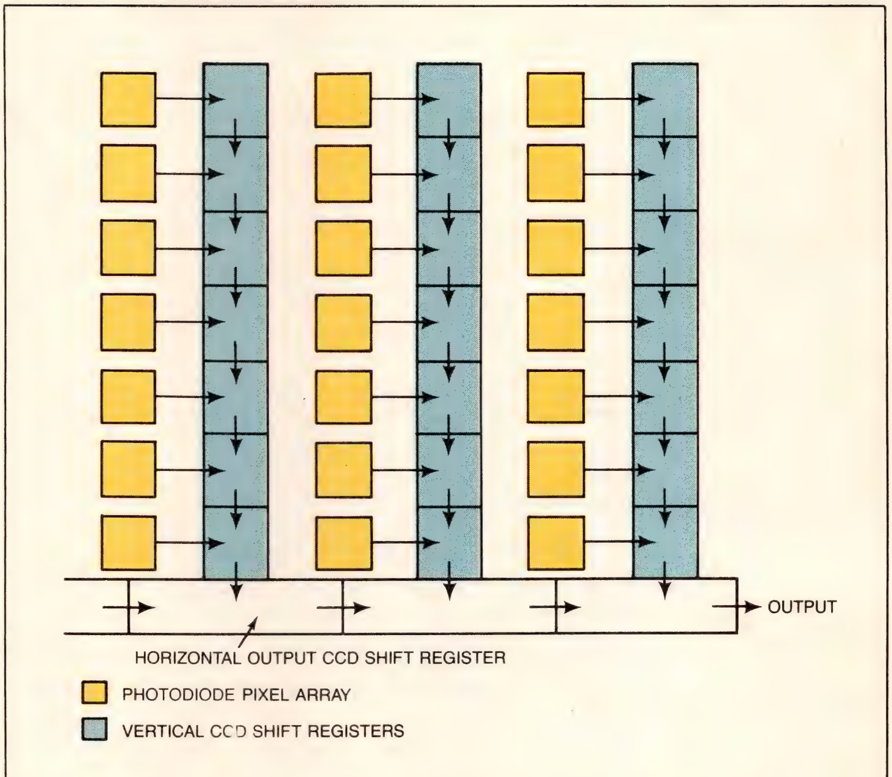


***Fig 1—In the interline-transfer arrangement,*** *the photosensitive elements are photodiodes and the scanning circuitry consists of light-shielded CCD analog shift registers. Like the arrangements shown in* ***Figs 2, 3,*** *and* ***4,*** *this one provides high resolution, but all differ in size of active imaging area, blue-end sensitivity, fixed-pattern and random noise levels, and scanning flexibility.*

different method of storing the pixel information and making it ready for output. These devices each consist of two identical arrays of CCD cells —one exposed to the image and used directly as the photosensitive array, and another shielded from incident light and used to store a complete frame of image information **(Fig 2).** During the vertical blanking interval, the entire frame is rapidly clocked from the imaging CCD array to the storage array. The output is generated during the succeeding frame period by shifting the storage area line by line into a horizontal output shift register and clocking it out serially. Because the CCD cells of the imaging area act directly as the photosensitive pixel elements, the only obscuration on the imaging area is the narrow channel-stop diffusion that isolates the vertical CCD shift registers from one another.

By generating two interlaced frames, Philips's NXA1010 and NXA1030 frame-transfer sensors achieve resolutions of 604×576 and 610×492 pixels (resolution specs give the horizontal dimension first). The former produces 625-line CCIR-standard TV outputs, and the latter, 525-line EIA-standard TV outputs. The NXA1020 and NXA1040 versions of the NXA1010 and NXA1030 include a color-stripe filter deposited onto the imaging array, which allows the devices to produce pal/Secam- or NTSC-compatible color outputs.

EEV's recently introduced P86000 and P85000 frame-transfer sensors also use two interlaced scans to produce resolutions of 385×576 and 385×488 pixels, respectively, for 625-line and 525-line TV outputs. Both Philips's and EEV's frame-transfer sensors use a true interlacing technique, which involves shifting the photosensitive area vertically by one line width for each successive frame scan. This action is accomplished by altering the drive waveforms to the CCD cells' electrodes.

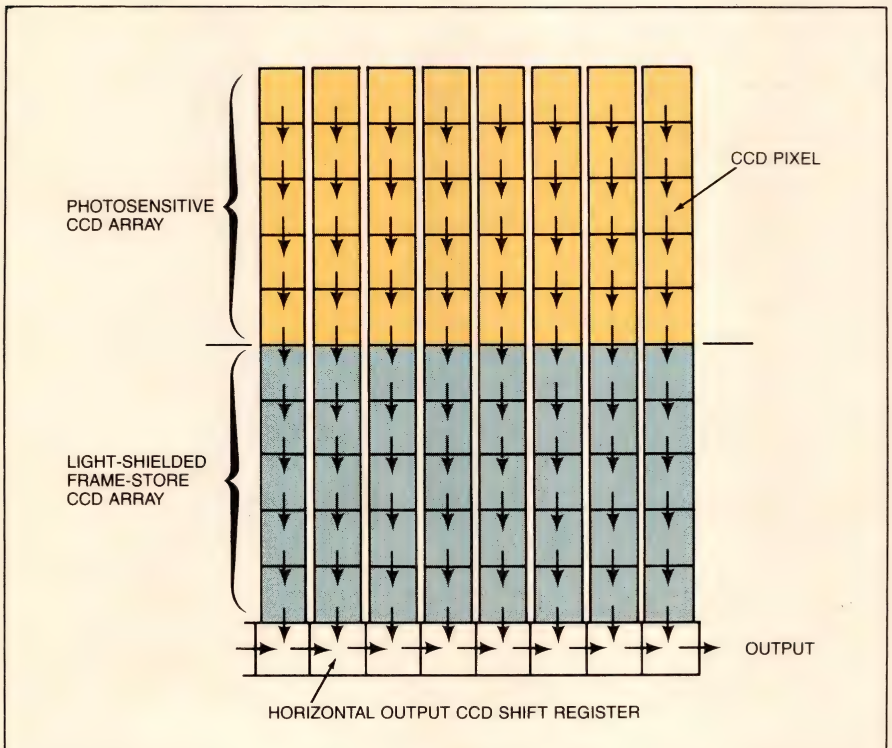


***Fig 2—Frame-transfer image sensors consist of two arrays of CCD cells.** One array is the photosensitive element, and the other composes the scanning circuitry. The latter stores a complete frame of image information, which is shifted line by line to the horizontal shift register for output.*

Texas Instruments, another supplier of frame-transfer CCD imagers intended as replacements for vidicon tubes, plans to introduce two products during 1986. The VID263 and the VID267 will provide resolutions of 192×165 pixels and 754×488 pixels, respectively. Both devices will conform to an 11-mm-diagonal format, and some versions will have integral color filters. The NTSC-compatible, high-resolution device, complete with a peripheral-chip set, is expected to sell for less than $100 when volume production starts in 1987.

### X-Y addressable arrays

Hitachi's area-scan image sensors use yet another technique for image readout. The photosensitive area consists of an array of photodiodes, each associated with a MOSFET switch and addressable in an X-Y matrix **(Fig 3).** The fabrication processes involved are similar to those used by the company to manufacture CMOS dynamic RAMs; this similarity contributes to lower manufacturing costs.

A vertical shift register and a horizontal shift register control the X-Y addressing. To scan the array, the vertical shift register turns on a complete row of MOSFETs by selecting one of the X-axis vertical gate lines. This action causes the photodiodes in the associated row to dump their integrated charge onto their corresponding vertical signal lines. The horizontal shift register then sequentially switches each vertical signal line to the output pin via a row of horizontal switch MOSFETs.

Hitachi's HE-97000 and HE-98000 product lines both include arrays compatible with NTSC and pal/Secam TV standards. The NTSC-compatible sensors employ interlacing and have 485 vertical pixels and as many as 576 horizontal pixels. Interlaced pal/Secam-compatible devices have 577 vertical

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pixels and 374 horizontal pixels. The products also include a 244×320-pixel noninterlaced array.

To build a machine-vision system capable of using the full resolution of vidicon-replacement image sensors, you'll probably have to design a custom camera. If you use the peripheral chips supplied by the vendor, you'll run into some limitations when interfacing the sensors' analog outputs to the digital circuitry of your computer. The scan-control and signal-conditioning ICs provided by the manufacturers of vidicon-replacement-type image sensors are usually designed to produce an RS-170 or similar standard composite-video output signal. Unfortunately, these signals are devoid of any clock information, other than relatively infrequent line-synchronization pulses, that would indicate precisely where in the analog output signal the center of each pixel is actually represented. As a result you don't know exactly where to perform an A/D conversion so that you can maintain an exact 1:1 relationship between the digitized samples and the corresponding pixel coordinate in the image sensing array—a particularly important requirement in noncontact measurement applications.

Even if you overcome this problem by driving the sensor's scan-control ICs and the image digitizer's A/D converter from the same clock source, you'll still have to contend with the signal delays introduced by the signal-conditioning circuitry. As a consequence, you'll be inclined to design your own signal-conditioning circuitry.

In applications where you don't need to push the limits of your device's resolution, you can usually provide adequate synchronization between the camera's scanning logic and the image-digitizing A/D converter by means of a phase-locked loop in either the camera or the digitizer. This facility is commonly referred to by camera manufacturers as Genlock.

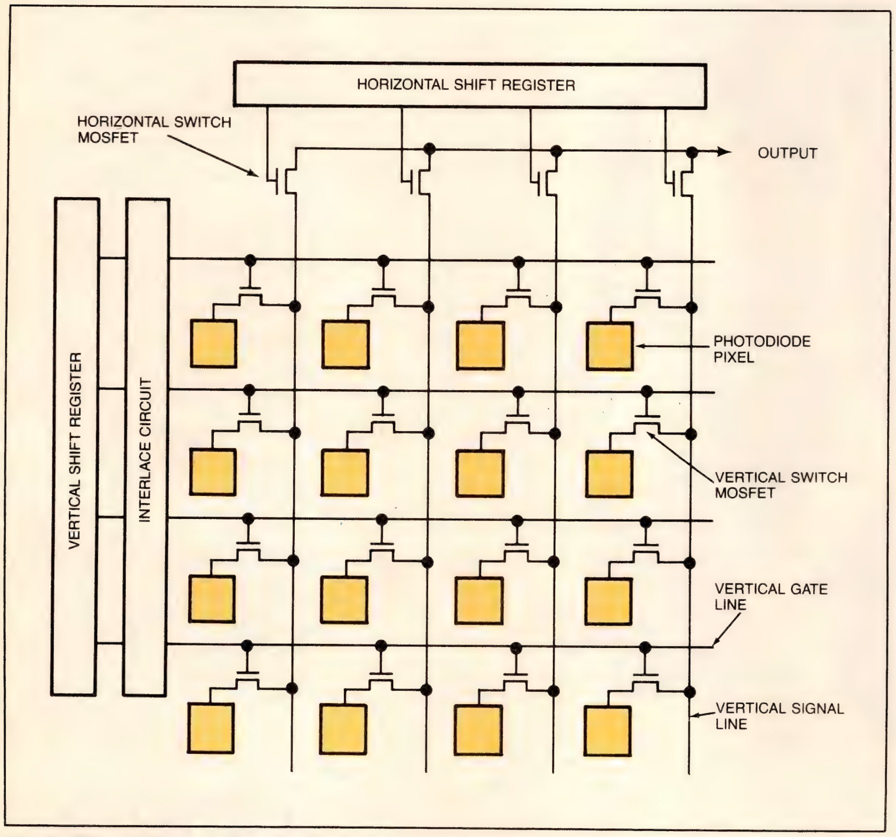


***Fig 3—The photosensitive area in this MOS X-Y image sensor*** *consists of a photodiode array arranged in an X-Y matrix. Each photodiode is associated with a MOSFET switch. The vertical shift register selects an X-axis vertical gate line, turns on a row of MOSFETs, and the associated photodiodes dump their integrated charge onto their corresponding vertical signal lines.*

### Structure limits blue response

The surface structure of solid-state image sensors also affects their blue-end spectral sensitivity. Short-wavelength radiation is rapidly absorbed by the polycrystalline silicon material typically used to fabricate the surface electrode structures of CCD-type image sensors. The result is poor sensitivity to incident wavelenths shorter than approximately 450 nm. Photodiode arrays, which have a greater proportion of exposed photosensitive silicon, tend therefore to exhibit higher blue-end sensitivities.

One way to overcome this shortcoming in CCD arrays is to thin down the underlying substrate material, typically to around 10 μm, and to illuminate the image onto the rear face of the sensor. Variants of EEV's P85000 and P86000 sensors feature this rear-face illumination.

Because vidicon-replacement-type image sensors are designed for use under uncontrolled lighting conditions, they have a wide dynamic range, typically 1000:1. Nearly all of today's devices also incorporate an antiblooming drain in the pixel structure to prevent excess charge in overexposed pixels from spilling over into adjacent pixels and whiting out areas of the image.

### TV standards limit exposures

The exposure times of image sensors oriented toward TV standards do, however, pose a problem. Because they are designed for 50- or 60-Hz field-scan rates and interlace two successive field scans to produce TV-standard 25- or 30-Hz frame rates, exposure times for the photosensitive arrays are typically 20 or 16.66 msec (40 or 33.3 msec in some cases). If you intend that your machine-vision system accept im-

ages of fast-moving objects, these exposure times will result in a blurred image. To eliminate this blurring you'll have to resort to an exposure-time-control mechanism—for example, strobed illumination of the object, or a mechanical or liquid-crystal shutter—all of which complicates the imaging system.

EEV's image sensors, built according to military specifications, go some distance toward alleviating the exposure problem by using a patented technique that involves reverse-clocking of the CCD array. While maintaining a 50- or 60-Hz field rate, this technique allows you to reduce the effective exposure time of the array from 20 msec to as little as 1 msec. Although the currently available peripheral ICs only allow you to choose 20-msec or 1-msec exposure times, you can add additional logic to provide several exposure steps in between these values—again, at the price of increased complexity.

Another drawback of these large area-scan arrays is that, unless you spend a lot of money, it's difficult to obtain devices that are free of blemishes, or fixed-pattern noise. It's more than likely that a few pixels in the array will exhibit reduced sensitivity or excessive dark current. In any of the image sensors that use CCD structures, either as their photosensitive pixels or as the scanning circuitry in conjunction with photodiodes, defects in the CCDs tend to affect all the charge packets that pass through them. Depending on where the defects are located, the result can be intensity streaks on the image. If you're analyzing the image at the single pixel level, you'll have to locate array defects and compensate for them in the system software.

## CID arrays suit automation

Although most solid-state area-scan image sensors are designed to replace vidicon tubes, not all of these parts are designed with TV standards in mind. General Electric employs a third image-sensor technology—the charge injection device (CID)—to produce a range of cameras that the company declares are better suited to industrial automation applications than are devices oriented to TV standards.

An X-Y grid of polysilicon row and column electrodes, separated from the underlying n-type epitaxial layer by a thin oxide layer, defines the individual pixels of the CID image sensor **(Fig 4).** It's common design practice to strap the upper row electrode with a narrow band of aluminum to improve noise performance and row-access speed. This design enhancement results in less than 10% obscuration of the photosensitive area.

The electrodes are normally biased so that a photon-induced charge generated in each pixel lies under the column electrode. In order to read a pixel, that pixel's column electrode is switched to a value below that of the row electrode, causing the charge to shift to the area beneath the row electrode. A current amplifier senses the resulting displacement current that flows in the row electrode. This current is proportional to the charge contained in the pixel. The current amplifier provides the sensor's output.

Vertical and horizontal shift registers sequentially select the row and column electrodes to provide line-by-line scanning of the array. At the end of each line scan, a row electrode is switched to its minimum potential, causing the stored charge to inject into the underlying substrate and thus clearing the pixel for the next charge-integration period.

Using this technology, General Electric produces arrays ranging in resolution from 128×128 to 512×776 pixels. Several of these arrays, together with their peripheral-control chips, feature the kind of electronic control of the scanning process that's desirable in machine-vision

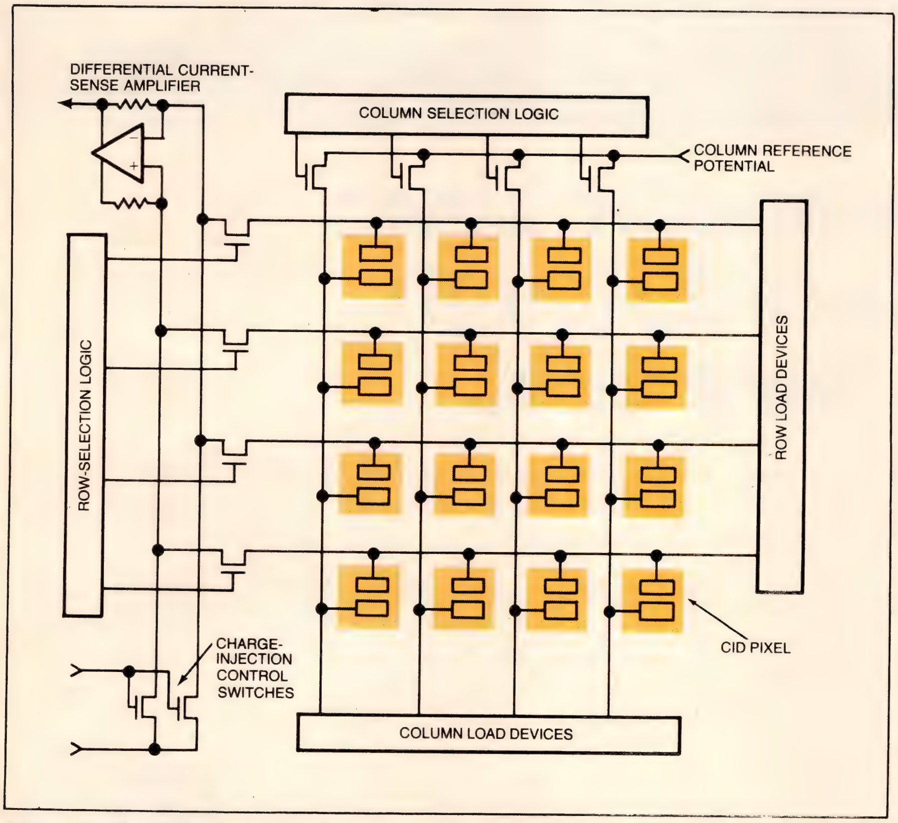


*Fig 4—**In the charge-injection-device (CID) image sensor,** an X-Y grid of polysilicon row and column electrodes defines the individual pixels. A thin oxide layer separates the electrodes from an underlying n-type epitaxial layer.*

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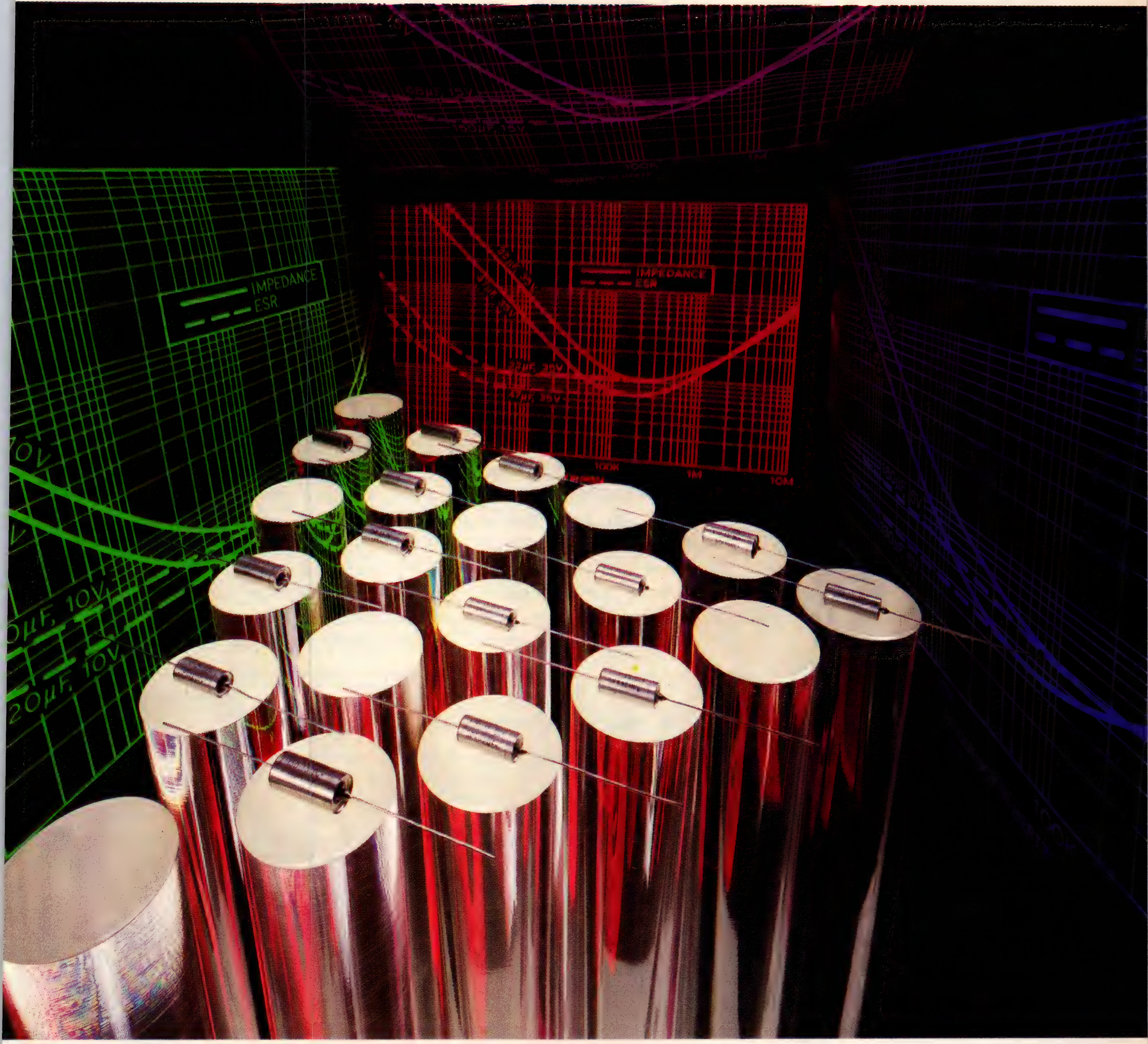


4SW-4129R1

# SPRAGUE TANTALUMS MEET MANY SMPS NEEDS.

Sprague Type 550D Solid-Electrolyte Tantalex® Capacitors, designed for use in power supply filters at frequencies to 100 kHz, feature extremely low ESR and high ripple current capability. Maximum ESR for a 300 $\mu$F, 6 VDC unit is only 0.045Ω at 100 kHz.

Additional advantages include small size, long life, exceptional capacitance stability and hermetic sealing to withstand severe environments. Capacitance values: 5.6 to 330 $\mu$F. Voltage ratings: 50 to 6 WVDC. *Sprague Electric Company, a Penn Central unit,* Worldwide Hdqtrs., Lexington, MA. Write for Engineering Bulletin 3548 to Technical Literature Service, Sprague Electric Co., 41 Hampden Road, Mansfield, MA 02048-1807.

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**CIRCLE NO 159**

systems. Features include the ability to clear the entire imaging array or to window onto selected areas of the array. In addition, the technology itself has some distinct advantages in these applications because it lends itself to random-access X-Y addressing and nondestructive readout of the image, which the company is currently working on. General Electric manufactures these devices primarily for use in its own range of automation and ENG cameras, but the company will supply subassemblies and components to volume users.

### Trade resolution for speed

If you're prepared to sacrifice resolution, then you can increase scan speeds and decrease corresponding exposure times. This choice entails that you go with one of the few solid-state area-scan image sensors that are not intended as replacements for vidicon tubes. EG&G Reticon produces self-scanned square-matrix photodiode arrays with resolutions ranging from 32×32 to 256×256 pixels. As an example of the tradeoff, the 256×256-pixel array, scanning at its maximum rate of 5 MHz, can produce approximately 76 frames/sec; the 100×100-pixel array produces 500 frames/sec at 5 MHz or 1000 frames/sec at its maximum rate of 10 MHz.

You can operate the EG&G sensors in interlaced or noninterlaced modes by modifying the clock inputs to the self-scan shift registers. A similar array family, the P87000 from EEV, has a 125×125-pixel photodiode array, with pixels on 40-μm centers to provide a 5-$mm^2$ image area. The P87000 scans at rates to approximately 150 frames/sec.

If you want to keep your costs to a minimum, you should consider the OpticRAM image sensors manufactured by Micron Technology. These sensors utilize the optically induced leakage current from a dynamic-RAM cell to provide single-

## For more information . . .

For more information on the solid-state image sensors described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

**English Electric Valve Company Ltd**
Waterhouse Lane
Chelmsford
Essex CM1 2QU, UK
(0245) 261777
**Circle No 717**

**EG&G Reticon**
345 Potrero Ave
Sunnyvale, CA 94086
(408) 738-4266
**Circle No 718**

**Ford Aerospace & Communications Corp**
Ford Rd
Newport Beach, CA 92660
(714) 720-6151
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**General Electric Co**
890 7th N St
Liverpool, NY 13088
(315) 456-2832
**Circle No 720**

**Hitachi America Ltd**
2210 O'Toole Ave
San Jose, CA 95131
(408) 435-8300
**Circle No 721**

**Micron Technology Inc**
2805 E Columbia Rd
Boise, ID 83706
(208) 386-3800
**Circle No 722**

**NEC Electronics Inc**
Box 7241
Mountain View, CA 94039
(415) 960-6000
**Circle No 723**

**Philips**
Elcoma Div
Box 523
5600 AM Eindhoven
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| **Harris:** 80C86<br>80C88 | **NEC:** V20<br>V30 | **RCA:** 1802<br>1805<br>1806<br>CDP6805C4<br>CDP6805D2<br>CDP6805E3 | **Signetics:** 8X300<br>8X305 |
| | | **Zilog:** Z80A<br>Z80B<br>Z80H<br>Z8001<br>Z8002 | **National:** NSC800 |

**...AND MORE.**

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***When constructed for rear-face illumination,** EEV's P86000 frame-transfer CCD image sensor achieves extended blue-end sensitivity. The sensor is available in versions for 525- or 625-line operation and has a horizontal resolution of 385 pixels.*

bit, on-chip digitization of an image. In addition, you can randomly access the pixel information. The IS32 OpticRAM, for example, provides you with two side-by-side photosensitive arrays, each with 128×256-pixel resolution, at a price of $42.

### Custom solutions

Finally, if standard parts don't satisfy your requirements, and you're willing to bear the cost, you can build a custom image sensor. Ford Aerospace and Communications will help you design a CCD image-sensing array with your specified surface structure, pixel size, and peripheral circuitry. In conjunction with Science Applications International Corp (San Diego, CA), the company has produced a 1024×1024-pixel array for use as part of an X-ray image-intensifier system for medical radiography. You'll also find that several companies mentioned in this article are prepared to couple their arrays with image intensifiers or fiber-optic assemblies for specialized applications. **EDN**

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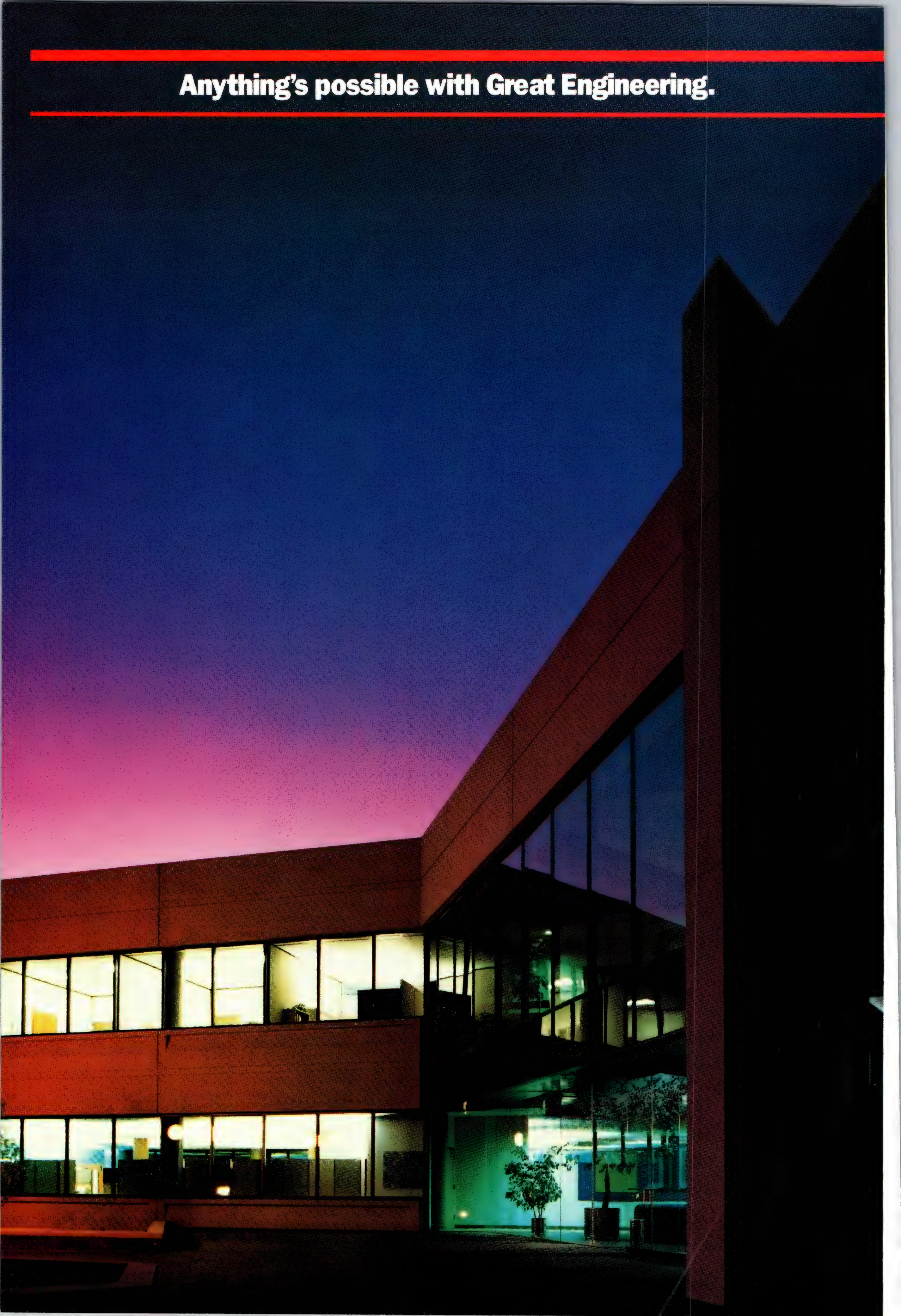
You can't be number one in semiconductors by making semicommitments.


Anything's possible with Great Engineering.

# GE Semiconductor. Anything's possible with Great Engineering.

General Electric's commitment to the electronics industry goes back to the first light bulb.

So we take it seriously.

Over the years, thousands of GE products have left our factories to take up jobs in military, telecommunications, computer and consumer applications.

Now our industry has reached the point where entire systems can be etched on a single microchip. And progress, for the foreseeable future, will clearly be spelled out in silicon.

So it should come as no surprise that GE is committed to the semiconductor industry. We're in it for keeps. And we've set a goal for ourselves.

Our goal is, simply, to be the most innovative, most respected semiconductor supplier in the world.

**We invested millions in a new plant. And gave it 110 acres to grow on.**

One of our first decisions was to build a new semiconductor facility that could become the focus of all our efforts. We decided to build on 110 wooded acres in Research Triangle Park, North Carolina. Right in the middle of the largest concentration of PHDs—and college basketball powers—in America.

Then we started recruiting. Not point guards and power forwards, but researchers, engineers and key executives from across the country. The line-up we began to assemble in the early '80s is now backed by so many advanced degrees, so much talent and experience, that we're deep in every position.

Our next move was to establish ourselves where the semiconductor industry has achieved so many of its breakthroughs: Silicon Valley and Boston's Route 128. In 1981, we acquired Intersil and Datel.

Intersil enhanced our ability to design complete analog/digital systems and execute them with the latest CMOS technology. It widened our product range with a respected portfolio in signal processing, A/D and D/A converters, analog switches and multiplexers, display drivers, microperipherals, digital controls and sophisticated linear circuitry.

We immediately opened an R&D center in Santa Clara and built and equipped a new Intersil facility in Cupertino. Armed with its new resources, Intersil advanced industry capability in monolithic ICs to 14 bits with our new 7115 14-bit high speed A/D converter. It gives you 25,000 conversions per second.

Intersil is also a major part of GE's effort to develop revolutionary new processing techniques. One of these, the 200-Volt CMOS process, is already operational, producing a new generation of analog switches, which expands applications.

In final stages, is a next-generation, silicon-gate/NPN bipolar mixture. With this BiMOS process, it's now feasible to design very low noise analog devices that are clearly superior to existing designs. And later this year, a radically new 1.5-micron VLSI process for high performance signal processing and high speed data conversion will be in volume production.

The addition of Datel contributed another 600 talented players, pioneering work in data acquisition products and experience in monolithic CMOS and bipolar, thin and thick film hybrids and discrete component circuits. Its product lines include data converters, sample-hold amplifiers, analog multiplexers, amplifiers, data acquisition subsystems, computer analog I/O boards, digital panel meters, panel printers, digital calibrators and power supplies.

Meanwhile, in North Carolina, we were reminding our people that anything's possible by outfitting our new facility with everything imaginable. Today every inch is so thoroughly engineered, even the window shades respond to light sensors. And there are enough clean rooms, laboratories and 5-inch wafer fab systems to accept any semiconductor challenge.

## We've spent 3 years and $4 million to put our custom/semicustom capability on military alert.

If any group of design engineers can understand and respond to our "anything's possible" philosophy, it's the military. As one of our biggest customers for high performance, high reliability components, they've seen its very pragmatic results.

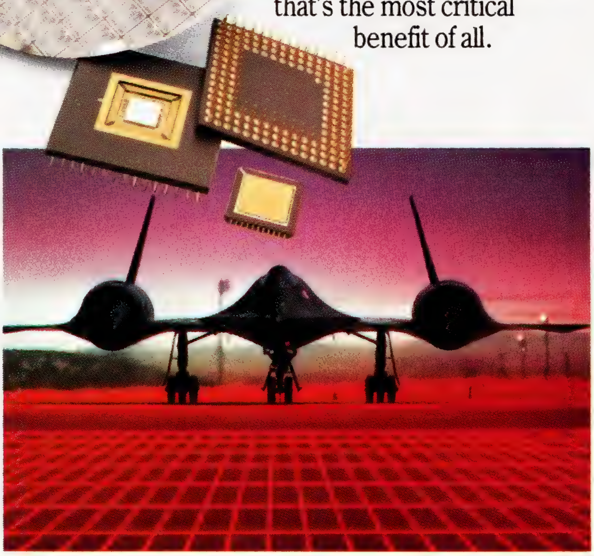
Now we're investing heavily to bring *all* our product lines into compliance with Military Standard 883, Revision C. And we're having all our test facilities, wafer fab systems and assembly lines undergo Defense Electronic Supply Center (DESC) certification.

But our military strategy goes far beyond qualifying individual components. Our objective is Joint Army-Navy (JAN) certification of all of our capabilities as a military semicustom supplier.

Once we're JAN-qualified, our engineers can bring all the advantages of application specific ICs to military systems. Designers' imaginations will face fewer restrictions. Circuits can contain more functions. And costs will drop for everything from design, through prototyping and manufacture.

By controlling the entire design and manufacturing process, GE will maintain the highest standards of quality.

The result will be far greater reliability. And, when the eventual application is the nation's defense, that's the most critical benefit of all.



## While the government funded VHSIC research, we completed AVLSI development.

The military vividly demonstrated its commitment to high technology when it funded research into the development of the Very High Speed Integrated Circuit (VHSIC). The goal was a 1.25-micron process with on-chip clock speed of 25 MHz.

Although GE Semiconductor wasn't funded for VHSIC research, its goals were far too important for us to sit it out. So we funded research of our own.

We combined the forces of GE Aerospace and GE Corporate R&D and began work on our VHSIC-compatible Advanced Very Large Scale Integration (AVLSI) program.

The results to date demonstrate that anything is indeed possible at GE Semiconductor.

While our competition continues to work on VHSIC processing, we've designed, prototyped and are now producing 1.25-micron CMOS, two-level metal gate arrays holding 10,000 gates. And our current process features 1.1-micron effective gate lengths, typical flip flop toggle rates of 175 MHz and gate delays of 750 picoseconds.

What's more, we'll begin full scale manufacturing of AVLSI circuits in early 1987.

To make it easy for you to work with AVLSI, we're making conversion from 2.0 to 1.25 microns a pushbutton process. And we're stretching our lead in the important area of user design software, such as silicon compilation.

The point is, at GE Semiconductor, AVLSI technology is ready. And waiting for you.

**The technologies we've developed for our sister companies are not for sale. They're free.**

While updating our facilities, we didn't forget to update what's even more important: our thinking.

In semiconductors, updated thinking means you don't manufacture chips and then find someone to buy them. Today supplying semiconductors really means supplying semiconductor *resources*. It means throwing open your doors and inviting people in who need a standard cell, a gate array or something else they're still "imagineering."

At GE Semiconductor, we can provide all the latest in CAE tools, training, service and manufacturing technology. We don't think anyone can match our resources.

And we've developed leadership product lines ranging from metal oxide varistors, power MOSFETs, optoelectronics and sophisticated signal processing ICs, to gate arrays, hybrids and standard cells.

But that's not all. We also offer a 100-year tradition of making the impossible *work*. We've spent millions of dollars and man-hours inventing technologies for other GE divisions. You can tap into all that experience, the full impact of that investment, at any GE Semiconductor facility or design center.

A good example of what this can mean is a new GE technology called GE-Smart™ intelligent power subsystems.

With 65% of the world's electricity going to power motors, several GE divisions were interested in making those motors smarter, more efficient, more reliable and quieter. But the problem has always been integrating logic and power functions in a cost-effective fashion.

GE engineers found a way. And it's going to find its way into GE appliances, GE engines, GE products of every description.

But it will also find its way into hundreds of non-GE products as well. Because GE Semiconductor engineers are going to help put it there.

Of course, we're not doing this out of sympathy for our competition. We're doing it because the market for smart power will grow to $1 billion by 1995. And that's just good business.


**We've moved 100 people 700 miles so you can put power and logic on the same chip.**

Perhaps GE was first to put power and logic on the same chip because we were first to put power and logic engineers in the same building. In fact, we're moving our entire power semiconductor operation in Syracuse, New York to Research Triangle Park.

We happen to think the people who made the first rugged power MOSFETs should work alongside the people making 1.25-micron gate arrays. And the CAD/CAM researchers from GE Calma should have lunch with the Silicon Systems Technology Department. They're working on advanced graphics processors and investigating ways to convert software algorithms into systems solutions.

Who knows what they'll sketch out on their napkins.

The important thing from your perspective, however, is this. Whatever they develop is yours for the asking. Better yet, you can sit down with them and conjure up a gate array or new application of your own.

By the way, you don't have to be working in the U.S. to work with GE. Our sales and service offices circle the globe. And we're establishing design centers in Europe and the Far East to complement our manufacturing affiliates in Ireland and Singapore.

# Whatever you need, wherever you are, anything's possible with Great Engineering.

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**Intersil, Inc.,** 10600 Ridgeview Court, Building 4, Cupertino, CA 95014, (408) 996-5000

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## GE Semiconductor Sales Headquarters

**North America**
GE Semiconductor Sales Department, One Micron Drive
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GE Semiconductor Sales Department, 150, Chausee de la Hulpe, Bte. 5, B-1170 Brussels, Belgium, (02) 660-2014

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**Hong Kong**
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20 Austin Ave., Tsimshatsui
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233075

IGE (India) Ltd., Archana Office Complex, Greater Kailashil
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**Italy**
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03-779-0401

**Korea**
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**Spain**
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Juan Bravo No. 3C
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**Sweden**
International General Electric, AB (Kistagangen 19), Box 1203, 163 13
Spanga, Stockholm, Sweden
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**United Kingdom**
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**United Kingdom**
Datel, Basingstoke, Belgrave House, Basingview, Hampshire RG 21 2YS, (256) 469085, TLX (851) 858041
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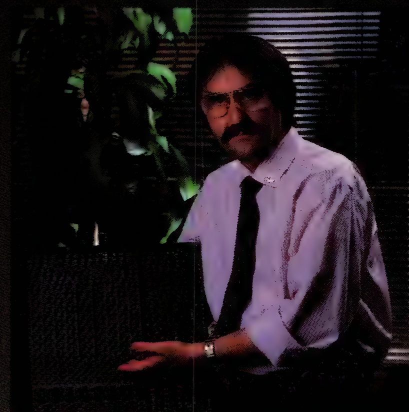
## Manufacturing Affiliates

Electronic Components of General Electric (USA) Private Ltd. (ECOGE), 105 Boon Keng Road 03-01, Singapore, 1233, Singapore

ECCO, Limited, Demesne, Carrick Road, Dundalk, County Louth, Ireland

GE Semiconductor

# Time May Be Running Out...



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**Where The Only Constant is Change, You Need Calay**

With the Calay system every aspect of the design cycle is accelerated including the rough spots such as the unexpected but inevitable engineering change orders. Calay makes initial data

# CPU/peripheral-controller ICs reduce cost, board size of PC bus-based 1-board systems

Two highly integrated CMOS CPU/peripheral controller ICs—the FE2010 and the FE3000—can reduce the board size and cost, lower the power requirements, and increase the reliability of IBM PC/AT bus-based systems. Originally incorporated into the manufacturer's own line of PC and PC/AT motherboards, both devices work in conjunction with a PROM-based BIOS, so they provide complete IBM PC compatibility.

The FE2010 PC Bus CPU/peripheral controller IC replaces 71 components, including Intel's 8284 clock generator, 8288 bus controller, 8259A interrupt controller, 8237A DMA controller, and 8253 timer. It handles four DMA, eight interrupt, and three timer channels, and it supplies complete CPU controller logic and a keyboard port. A system-configuration register eliminates external switches.

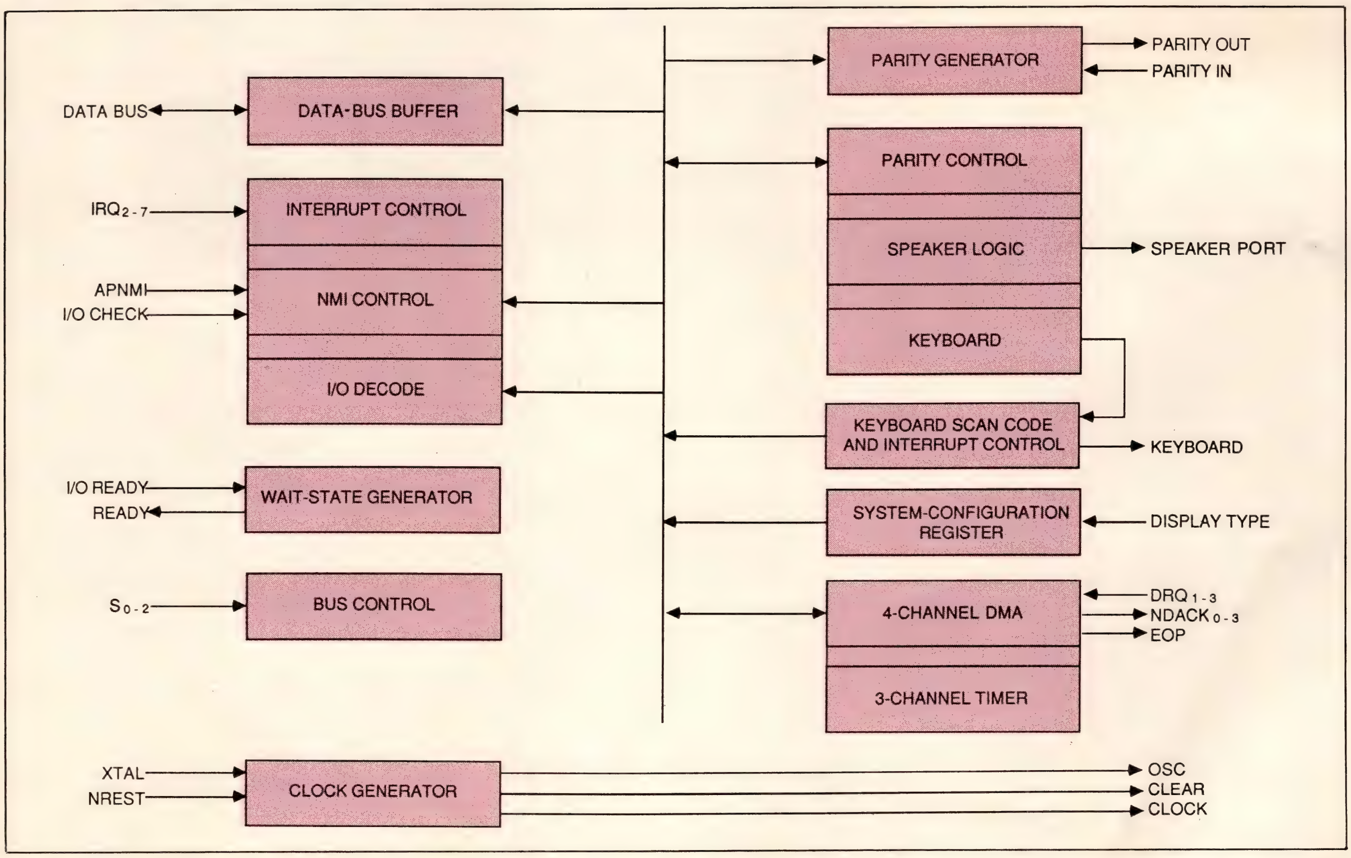
The FE3000 PC/AT bus controller is compatible with Intel's 16-bit 80286 processor and upwardly compatible with its 32-bit 80386 CPU. The controller integrates 53 components, including nonmaskable interrupt (NMI) and DMA control logic, an 8284/82284-compatible clock generator, and an 82288-compatible bus controller. It supports 6-, 8-, and 10-MHz clock speeds and can accommodate 256k- and 1M-bit dynamic RAMs.

Both controllers are 2-μm CMOS ICs that come in 84-pin J-leaded surface-mount plastic chip carriers. Prices for the FE2010 and FE3000 are $76 and $45 (100), respectively. The PC BIOS costs $25, and the PC/AT BIOS sells for $35 (100); both require a $15,000 licensing fee. The manufacturer also offers the FE2100 floppy-disk controller IC for $13 and the FE2200 monochrome display controller IC for $34 (100). Delivery, 12 weeks ARO.

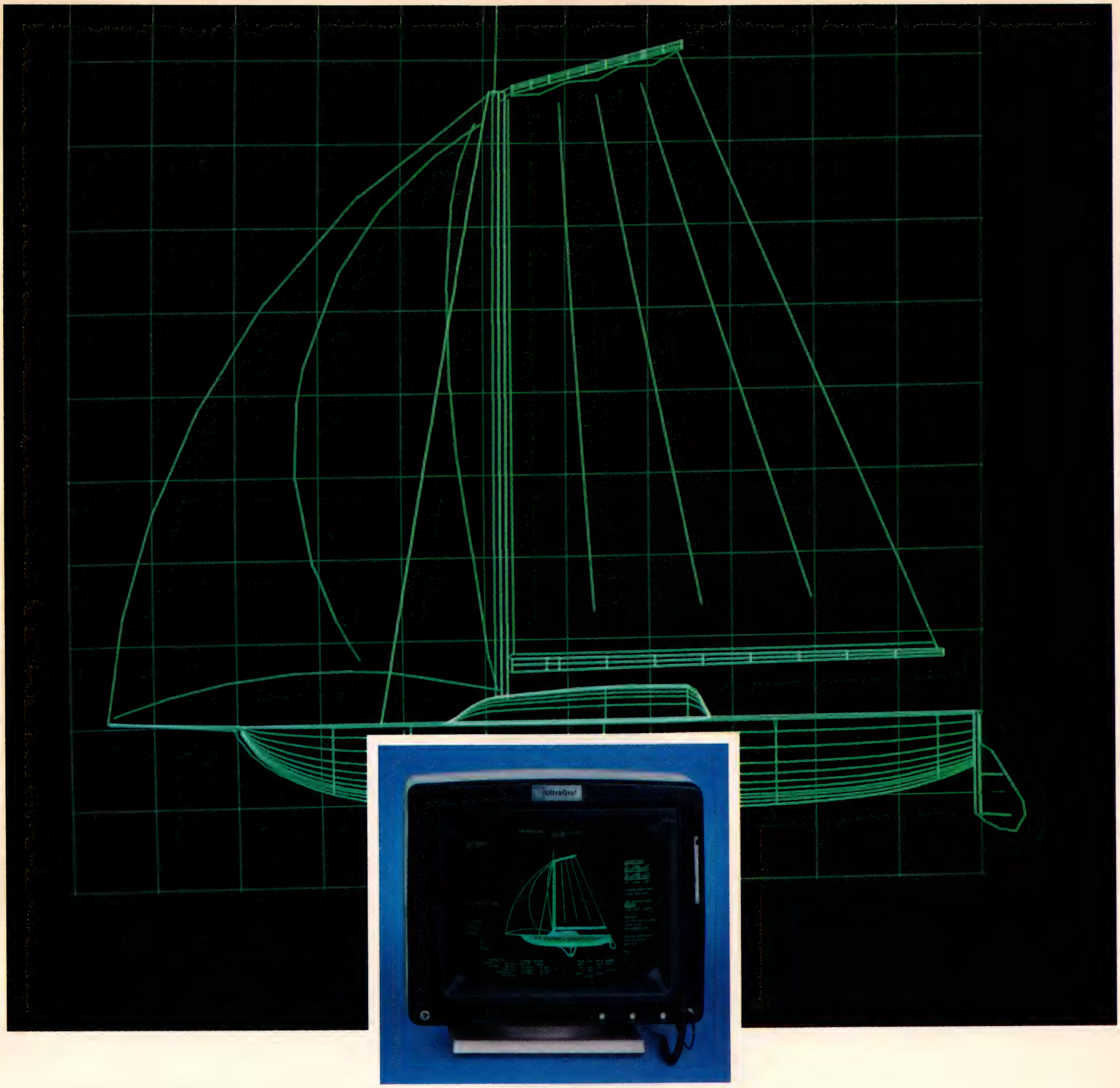
***—Margery S Conner***

*Faraday Electronics, 743 Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 749-1900.*

**Circle No 727**




***Replacing 71 components,*** *including Intel's 8284 clock generator, 8288 bus controller, 8259A interrrupt controller, 8237A DMA controller, and 8253 timer, the FE2010 PC bus-based CPU/peripheral controller IC can reduce board space by 77%.*



# Designing Is a Breeze with Lundy's New UltraGraf® II

No matter what business you're in, sluggish productivity could blow you—and your profits—away. But now, thanks to Lundy's new UltraGraf® II, there's an economical way to fight back. UltraGraf® II is an intelligent 3-D graphics workstation with features and functions that help you breeze through intricate designs.

**Exceptional Quality and Performance**

What sets UltraGraf® II apart from other workstations in its price range is its exceptional quality and performance. That's because Lundy engineers have developed extremely efficient vector and hardware processors that permit fast, high resolution design. And unlike many other workstations, UltraGraf® II is highly intelligent. So functions such as 3-D translation, rotation, and scaling are performed locally, increasing design speed even further while freeing your host. The result is fast, high quality design that helps keep rigid development schedules firmly on course.

A wide variety of options and accessories are available to help make graphics design as convenient as possible. And as with all Lundy products, UltraGraf® II is backed by our customer service and support network, one of the largest in the industry.

This combination of speed, intelligence, responsiveness, economy, options, accessories, service and support make UltraGraf® II the ideal choice for mechanical design and drafting, architectural engineering, finite element analysis, robotics, and other applications that require high resolution display.

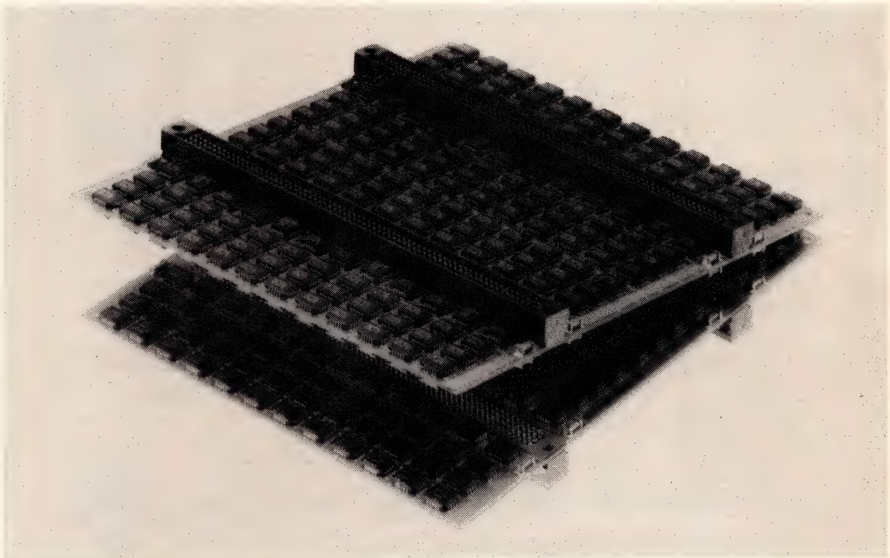
So don't let sluggish design productivity take the wind out of your sails. Fight back with UltraGraf® II.

Contact: Graphics Marketing, Lundy Electronics & Systems, Inc. 1 Robert Lane, Glen Head, N.Y. 11545 (516) 671-9000.

LUNDY®

CIRCLE NO 152

# Unix workstation employs 32-bit CPU, offers 1280×1024-pixel graphics



*Surface-mount devices squeeze 64M bytes of RAM* onto one double-sided memory board, which fits into the Edge1 workstation's deskside cabinet.

Edge1 engineering workstations deliver 3.5 MIPS (performance that's roughly equivalent to that of a VAX 8600 computer), but cost between $48,000 and $100,000 (100) with graphics hardware and Unix. An Edge1 system with 64M bytes of RAM, a graphics engine, and a floppy-disk drive resides in a deskside cabinet. To expand the system's I/O capability, you can put plug-in VME Bus or Multibus cards into the cabinet.

The manufacturer uses a proprietary CPU engine to fit a supercomputer architecture into the deskside cabinet. The extensive use of CMOS gate arrays eliminates the need for special cooling equipment. The 32-bit CMOS CPU accesses data and memory separately, allowing each memory fetch to access 64 bits of data. Pipelines buffer data and memory; branch-prediction hardware helps keep the pipelines full. A floating-point processor (optional on monochromatic systems) implements IEEE-754 floating-point standards.

The company claims that for a variety of programs, including scalar multiplication, Unix routines, and CAE software, the workstations deliver as much as four times the performance of a DEC VAX 11/780, which puts them into the same performance class as the DEC VAX 8600 superminicomputer.

An Edge1 workstation includes a system bus for local processing and a peripheral bus for expansion boards. An MMU manages memory transactions over the 80M-byte/sec system bus. You can order a workstation with either a VME Bus or a Multibus chassis; you can add either six (VME Bus) or seven (Multibus) boards to the system. Aggregate I/O bandwidth is 16M bytes/sec.

The workstations can include as much as 64M bytes of RAM. Using dual-sided surface-mounted technology, the company puts the entire memory onto one board, which fits into the deskside cabinet.

Each workstation comes with a complete graphics subsystem that implements some graphics functions in hardware. A window-manager circuit supports applications requiring a user interface. A Gouraud-shading circuit fills in the surfaces of solid figures, and a 16-bit buffer stores hidden (z-axis) surfaces. The subsystem can process 28,000 3D-polygons/sec and 30,000 text characters/sec. In addition, the Edge1 workstations come with color or monochromatic monitors that deliver 1280×1024-pixel resolution and 60-Hz, noninterlaced displays. You can display 4096 colors simultaneously from a palette of 16.8 million colors.

For storage, the workstation comes with a floppy-disk drive and the capability of supporting as many

***Graphics, Unix, and 3.5-MIPS performance*** *fit into the deskside cabinet of an Edge1 workstation. The cabinet also has room for six VME Bus boards or seven Multibus boards.*

# UPDATE

as seven hard-disk drives. Because the workstation can operate with 80M-, 165M-, 330M-, and 500M-byte disk drives, you can add as much as 3.5G bytes of disk storage to the system.

For I/O operations, the workstations provide four RS-232C ports, and you can add more ports in groups of four. Optionally, you can order an Ethernet TCP/IP LAN connection. You can also add any other type of I/O that you can find on VME Bus or Multibus boards.

The systems come with a guaranteed-share Unix operating system (a derivative of Unix System V) that lets you set resource allocation for programs sharing the workstation. The systems also include compilers for C, Pascal, and Fortran 77.

Edge1 workstations are available in four configurations. You can order the basic configuration (2M bytes of RAM and 80M bytes of disk storage) with a monochromatic monitor for $48,000 (100). A color workstation starts at $58,000, and a system configured as a computational server starts at $44,000 (100). The company also offers the Edge1 as a 64-user Unix system for between $60,000 and $99,000 (100). All system prices depend on memory and installed-disk capacity; discounts for larger quantities can reach 42%.—***David Smith***

*Edge Computer Corp, 7273 E Butherus Dr, Scottsdale, AZ 85260. Phone (602) 951-2020.*

**Circle No 726**

# TAKE THE TOUR

You hear so much about **PCB CAD SYSTEMS** these days, now here's a chance to see what a CAD SYSTEM can do...take the **QUIK CIRCUIT™** GUIDED TOUR from Bishop... Only **$15.00**

erybody claims to have a CAD system at'll make your life as a printed circuit ard designer easier. But talk is cheap. With shop's low-cost QUIK CIRCUIT PCB D/CAM system you can sample its time and ork saving benefits *before* you buy. Bishop vites you to take the *QUIK CIRCUIT Guided ur.* The Tour (a demonstration diskette and nchronized audio tape) takes just 35 inutes. And you can make stops along the ay to put QUIK CIRCUIT through its paces, d try its easy-to-use features yourself.

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u'll be impressed with how easy it is to use UIK CIRCUIT – *no typing expertise quired...no dozens of commands to emorize.* You'll also be impressed with how owerful it is – *multi-layer capabilities; rface mount technology (SMT); board sizes p to 32″ X 32″; finished artwork, brication and assembly documentation at X, 2X and 4X.*

nd QUIK CIRCUIT is flexible. Create hatever pads, patterns and traces you need complete your layout...*your library of lements is unlimited!* And design changes, hich can be made at any time, re a snap.

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Like the QUIK CIRCUIT software, the demonstration diskette runs on an Apple Macintosh 128K, 512K or XL personal computer, an Apple Lisa system with MacWorks, and the powerful new Macintosh Plus.

The QUIK CIRCUIT Guided Tour (Order No. 30008) is available now from your local authorized Bishop Graphics CAD Systems dealer for only $15.00. Call Bishop Graphics CAD System Corporation **TOLL-FREE at 800-222-5808** (in Alaska, Hawaii and California, call 818-991-2600) for the name of your nearest dealer.

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CIRCLE NO 71

# Monolithic synchronous V/F converter is first to guarantee 0.005% linearity

By using an external clock to set the desired full-scale output frequency, the AD651 synchronous V/F converter (**Fig 1a**) eliminates the errors introduced by the external passive components that nonsynchronous units require. Although you must connect an external integrating capacitor ($C_{INT}$ in **Fig 1b**), the characteristics of this capacitor do not affect the device's transfer function. For a 0 to 10V input-voltage range, the transfer function is

$$f_{OUT}=(V_{IN}\times f_{CLOCK})\div 20V,$$

where $f_{CLOCK}$ is 4 MHz max. The maximum output frequency is thus 2 MHz.

The AD651 outperforms any other monolithic V/F converter. Its closest rival is the VFC100 synchronous V/F converter, a device that also accepts clock frequencies as high as 4 MHz, but whose data sheet specifies performance for full-scale output frequencies only as high as 1 MHz.

Linearity specs for the best-grade VFC100 are 0.025%, 0.05%, and 0.1% max for full-scale output frequencies of 100 kHz, 500 kHz, and 1 MHz, respectively. The best-grade AD651 specifies 0.005% max nonlinearity for all three frequencies and 0.02% max for a 2-MHz FS output range. A lower-grade AD651 specs 0.02% max nonlinearity for the three frequencies and 0.05% max for a 2-MHz FS output range.

Gain-error and -drift specs constitute another strong point of the AD651. The best-grade AD651 specs 0.5% max gain error and 25-ppm/°C max gain drift for 100- and 500-kHz FS outputs, and 0.75% and 50 ppm/°C max for a 2-MHz FS output. (Corresponding gain-error and -drift specs for the best-grade VFC100 are 0.5% max gain error and 50-ppm/°C max gain drift for a 100-kHz FS output; the part has no specs for higher frequencies.) Gain error for the relaxed-spec AD651 is 1% max for the 100- and 500-kHz ranges, and 1.5% max for the 2-MHz range. Gain drift for the part is 50 ppm/°C max for the 100- and 500-kHz output ranges, and 75 ppm/°C max for the 2-MHz range.

The only external components you need to operate the AD651 are integrating capacitor $C_{INT}$ and a 1N4148 or 1N914 diode. The diode (which is opaque to prevent light-induced changes in characteristics) is connected between the inverting and noninverting inputs of the input amplifier. It prevents fault conditions from forward-biasing any of

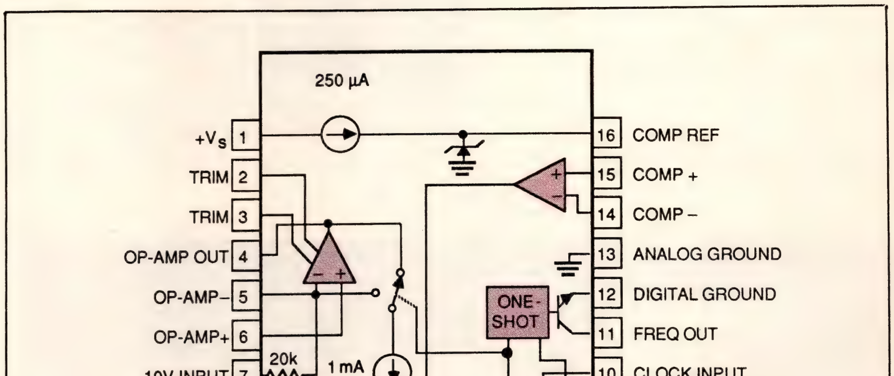



*Fig 1—**Immune to the characteristics of external components,** the AD651 synchronous V/F converter **(a)** uses an external clock to set its full-scale output frequency. $C_{INT}$ **(b)** is the device's externally connected integrating capacitor; $C_{OS}$ sets the width of the pulses the one-shot produces. If you eliminate $C_{OS}$ entirely, the AD651 produces pulses approximately 100 nsec wide.*


***Unequivocally the most linear monolithic V/F converter available,** the AD651 synchronous V/F converter from Analog Devices has specs that guarantee 0.005% max nonlinearity for a 1-MHz FS output frequency.*

the IC's internal parasitic junctions.

Except for its need for the external diode, the AD651 is drop-in compatible with the VFC100. Note, however, one other difference between the two units: The VFC100's comparator-reference voltage at pin 16 is a buffered 5V; the AD651's is an unbuffered 6.8V. In applications in which pin 16 connects only to the pin 15 comparator input, this difference does not compromise compatibility.

$C_{OS}$, an optional external component **(Fig 1b),** controls the width of the output pulses coming from the one-shot multivibrator. In the absence of $C_{OS}$ (pin 9 open), the pulse width is approximately 100 nsec; if you use the capacitor, the pulses widen at the rate of about 5 nsec/pF. You can disable the one-shot by connecting pin 9 to $+V_S$; the output's pulse width is then equal to the clock period.

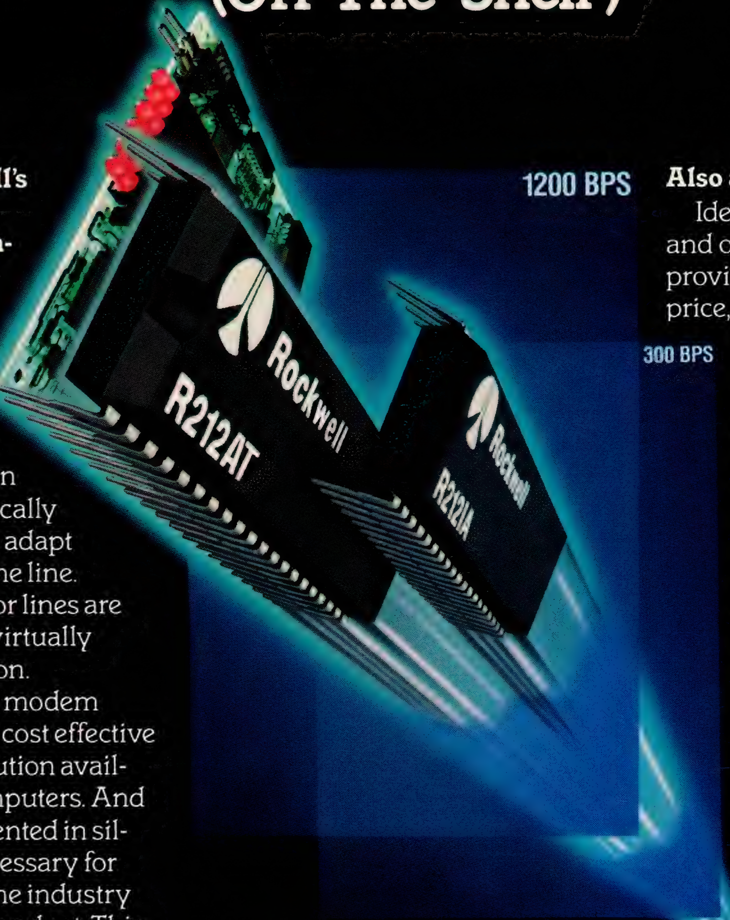
Capable of operating from a single 12 to 36V supply or from dual supplies ranging from ±6 to ±18V, the AD651 draws ±9-mA typ, ±15-mA max quiescent current. (The VFC100 is not specified for single-supply operation.) Housed in a 16-pin ceramic DIP, the AD651 is available in versions that operate over −25 to +85°C or −55 to +125°C; units screened to MIL-STD-883 are also available. Prices for the converter range from $7.95 to $18.50 (100).—***Bill Travis***

*Analog Devices Semiconductor, 804 Woburn St, Wilmington, MA 01887. Phone (617) 935-5565.*

**Circle No 728**

# ROCKWELL SEMICONDUCTOR TECHNOLOGY DELIVERS 1200 BPS AT 300 BPS PRICES.

## (Off-The-Shelf)



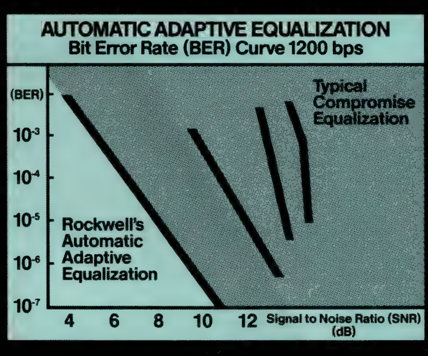

**Introducing Rockwell's new R212AT smart modem device set featuring Automatic Adaptive Equalization.**

Rockwell International's exclusive Automatic Adaptive Equalization Algorithms automatically enable the modem to adapt to any quality of phone line. Even signals over poor lines are enhanced to ensure virtually error-free transmission.

The R212AT smart modem device set is the most cost effective communications solution available for personal computers. And R212AT has implemented in silicon the software necessary for compatability with the industry standard "AT" command set. This allows quick design-in because we've presolved all the "AT" dialing functions. It incorporates auto dial, auto answer and can dial DTMF tones or pulses.

The R212AT smart modem offers lower system cost because it incorporates the controller and analog filter circuitry required for modem communications in the device set itself. This reduces parts count, enhances total system reliability and meets low power requirements for portable applications.

As well as operating asynchronously, the R212AT has synchronous mode operation for higher transmission throughput.




**Also available: Rockwell's R212DP.**

Ideal for remote diagnostics and other integral applications, it provides specific advantages in price, performance and system cost savings.

The R212DP, like the R212AT, has automatic fall back to slower speeds and an RS232C interface. Both these Bell 212A and 103 compatible device sets are available at any level of integration from devices to boards or customized private label systems.

For ease of evaluation, Rockwell provides a board level evaluation modem for laboratory analysis to assure the performance and quality of R212AT and R212DP.

Call your local Rockwell distributor today for off-the-shelf delivery of an evaluation board complete with a Designer's Guide Kit.

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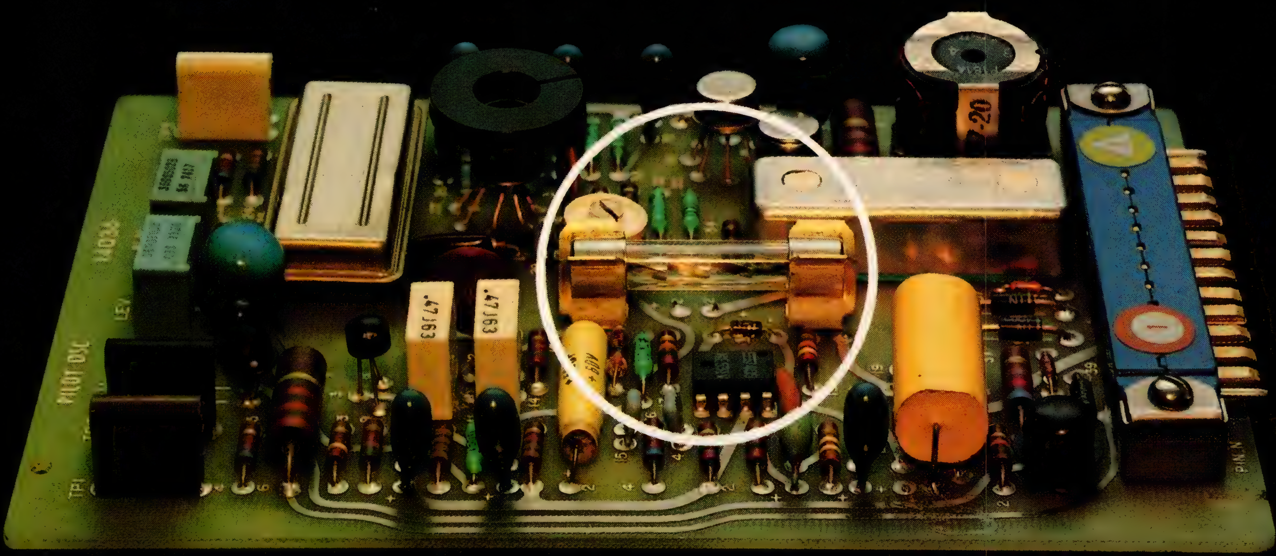
CIRCLE NO 153

# The fuse you must use, now:



# LEADTIME INDEX

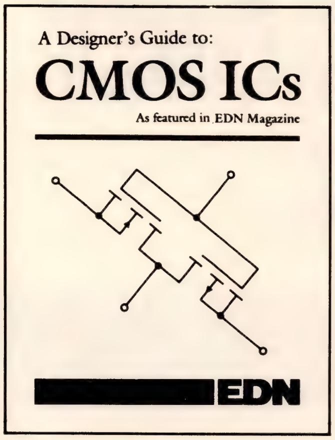
Percentage of respondents

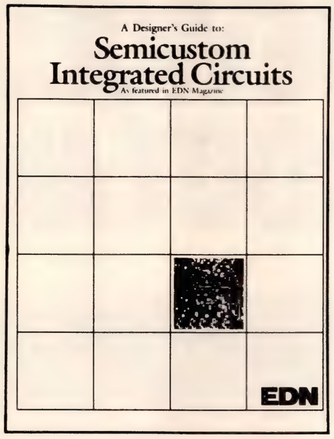
| ITEM | Off the shelf | 1-5 weeks | 6-10 weeks | 11-20 weeks | 21-30 weeks | Over 30 weeks | Average (weeks) | Last month's average (weeks) |
|---|---|---|---|---|---|---|---|---|
| **TRANSFORMERS** | | | | | | | | |
| Toroidal | 7 | 22 | 57 | 14 | 0 | 0 | 7.2 | 11.3 |
| Pot-Core | 8 | 23 | 46 | 23 | 0 | 0 | 7.8 | 9.3 |
| Laminate (power) | 0 | 14 | 72 | 14 | 0 | 0 | 8.3 | 8.4 |
| **CONNECTORS** | | | | | | | | |
| Military panel | 10 | 30 | 50 | 10 | 0 | 0 | 6.2 | 8.0 |
| Flat/Cable | 26 | 42 | 21 | 11 | 0 | 0 | 4.3 | 3.5 |
| Multipin circular | 13 | 20 | 47 | 13 | 70 | 0 | 8.1 | 7.6 |
| PC | 13 | 50 | 31 | 6 | 0 | 0 | 4.4 | 4.5 |
| RF/Coaxial | 13 | 53 | 20 | 7 | 7 | 0 | 5.6 | 5.6 |
| Socket | 29 | 48 | 14 | 9 | 0 | 0 | 3.5 | 3.4 |
| Terminal blocks | 17 | 46 | 29 | 8 | 0 | 0 | 4.5 | 3.7 |
| Edge card | 11 | 53 | 31 | 5 | 0 | 0 | 4.3 | 4.4 |
| Subminiature | 7 | 36 | 50 | 70 | 0 | 0 | 5.8 | 2.8 |
| Rack & panel | 10 | 40 | 40 | 10 | 0 | 0 | 5.6 | 5.6 |
| Power | 27 | 46 | 27 | 0 | 0 | 0 | 3.1 | 6.9 |
| **PRINTED CIRCUIT BOARDS** | | | | | | | | |
| Single-sided | 0 | 65 | 35 | 0 | 0 | 0 | 4.1 | 4.1 |
| Double-sided | 0 | 50 | 50 | 0 | 0 | 0 | 5.0 | 5.0 |
| Multilayer | 0 | 47 | 47 | 6 | 0 | 0 | 5.7 | 9.8 |
| Prototype | 10 | 80 | 10 | 0 | 0 | 0 | 2.4 | 2.0 |
| **RESISTORS** | | | | | | | | |
| Carbon film | 32 | 36 | 28 | 4 | 0 | 0 | 3.6 | 3.0 |
| Carbon composition | 29 | 29 | 38 | 4 | 0 | 0 | 4.3 | 5.2 |
| Metal film | 36 | 32 | 29 | 3 | 0 | 0 | 3.4 | 3.0 |
| Metal oxide | 21 | 36 | 43 | 0 | 0 | 0 | 4.2 | 3.7 |
| Wirewound | 22 | 35 | 35 | 8 | 0 | 0 | 4.9 | 4.7 |
| Potentiometers | 31 | 35 | 25 | 9 | 0 | 0 | 4.1 | 5.2 |
| Networks | 42 | 37 | 21 | 0 | 0 | 0 | 2.4 | 5.2 |
| **FUSES** | 57 | 17 | 17 | 9 | 0 | 0 | 3.1 | 2.5 |
| **SWITCHES** | | | | | | | | |
| Pushbutton | 34 | 33 | 22 | 11 | 0 | 0 | 4.2 | 4.7 |
| Rotary | 13 | 20 | 47 | 20 | 0 | 0 | 7.4 | 7.3 |
| Rocker | 25 | 34 | 33 | 8 | 0 | 0 | 4.6 | 6.3 |
| Thumbwheel | 8 | 59 | 25 | 8 | 0 | 0 | 4.5 | 9.8 |
| Snap action | 33 | 33 | 20 | 14 | 0 | 0 | 4.9 | 5.3 |
| Momentary | 7 | 57 | 22 | 14 | 0 | 0 | 5.1 | 5.8 |
| Dual in-line | 10 | 60 | 20 | 10 | 0 | 0 | 4.4 | 5.6 |
| **WIRE AND CABLE** | | | | | | | | |
| Coaxial | 39 | 59 | 11 | 0 | 0 | 0 | 1.9 | 3.2 |
| Flat ribbon | 45 | 36 | 14 | 5 | 0 | 0 | 2.6 | 1.6 |
| Multiconductor | 38 | 33 | 29 | 0 | 0 | 0 | 3.0 | 2.4 |
| Hookup | 58 | 32 | 10 | 0 | 0 | 0 | 1.4 | 1.7 |
| Wire wrap | 72 | 14 | 7 | 7 | 0 | 0 | 2.0 | 2.7 |
| Power cords | 27 | 32 | 32 | 9 | 0 | 0 | 4.6 | 3.2 |
| Other | 25 | 12 | 50 | 13 | 0 | 0 | 6.3 | 2.4 |
| **POWER SUPPLIES** | | | | | | | | |
| Switching | 0 | 41 | 47 | 12 | 7 | 0 | 6.5 | 8.4 |
| Linear | 6 | 50 | 25 | 19 | 9 | 0 | 6.0 | 8.7 |
| **CIRCUIT BREAKERS** | 6 | 35 | 30 | 29 | 0 | 0 | 7.7 | 7.8 |
| **HEAT SINKS** | 23 | 41 | 24 | 12 | 0 | 0 | 4.7 | 6.0 |

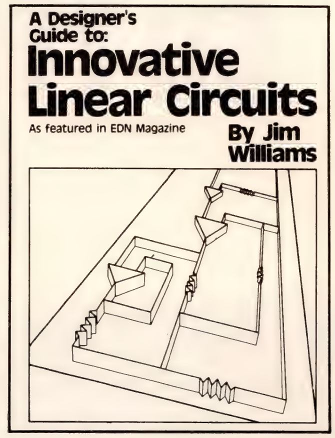
| ITEM | Off the shelf | 1-5 weeks | 6-10 weeks | 11-20 weeks | 21-30 weeks | Over 30 weeks | Average (weeks) | Last month's average (weeks) |
|---|---|---|---|---|---|---|---|---|
| **RELAYS** | | | | | | | | |
| General purpose | 29 | 24 | 33 | 14 | 0 | 0 | 5.4 | 5.0 |
| PC board | 13 | 27 | 33 | 27 | 0 | 0 | 7.5 | 7.6 |
| Dry reed | 0 | 46 | 36 | 18 | 0 | 0 | 6.7 | 6.0 |
| Mercury | 0 | 50 | 38 | 12 | 17 | 0 | 6.0 | 9.0 |
| Solid state | 9 | 18 | 46 | 27 | 8 | 0 | 8.3 | 8.8 |
| **DISCRETE SEMICONDUCTORS** | | | | | | | | |
| Diode | 29 | 32 | 26 | 13 | 0 | 0 | 4.8 | 5.5 |
| Zener | 34 | 31 | 21 | 14 | 0 | 0 | 4.5 | 4.8 |
| Thyristor | 24 | 29 | 29 | 18 | 0 | 0 | 5.8 | 6.1 |
| Small signal transistor | 31 | 17 | 35 | 17 | 0 | 0 | 5.9 | 5.7 |
| FET, MOS | 24 | 18 | 35 | 18 | 5 | 0 | 7.3 | 12.6 |
| Power, bipolar | 22 | 7 | 50 | 21 | 0 | 0 | 7.5 | 8.1 |
| **INTEGRATED CIRCUITS, DIGITAL** | | | | | | | | |
| CMOS | 20 | 32 | 32 | 16 | 0 | 0 | 5.8 | 7.4 |
| TTL | 22 | 30 | 26 | 22 | 0 | 0 | 6.2 | 9.0 |
| LS | 33 | 19 | 24 | 24 | 0 | 0 | 6.1 | 8.3 |
| **INTEGRATED CIRCUITS, LINEAR** | | | | | | | | |
| Communication/Circuit | 0 | 20 | 60 | 20 | 0 | 0 | 8.4 | 9.8 |
| OP amplifier | 10 | 32 | 37 | 21 | 0 | 0 | 7.0 | 8.1 |
| Voltage regulator | 14 | 34 | 33 | 19 | 0 | 0 | 6.4 | 7.2 |
| **MEMORY CIRCUITS** | | | | | | | | |
| RAM 16k | 7 | 40 | 20 | 33 | 0 | 0 | 7.7 | 8.0 |
| RAM 64k | 26 | 32 | 16 | 26 | 0 | 0 | 8.7 | 6.2 |
| RAM 256k | 7 | 29 | 43 | 21 | 0 | 0 | 7.4 | 7.8 |
| ROM/PROM | 8 | 17 | 42 | 33 | 0 | 0 | 9.0 | 8.0 |
| EPROM | 18 | 41 | 18 | 23 | 0 | 0 | 5.9 | 6.5 |
| EEPROM | 8 | 25 | 42 | 25 | 0 | 0 | 7.9 | 9.1 |
| **DISPLAYS** | | | | | | | | |
| Panel meters | 0 | 46 | 45 | 9 | 0 | 0 | 6.0 | 5.6 |
| Fluorescent | 0 | 0 | 57 | 43 | 0 | 0 | 11.4 | 6.5 |
| Incandescent | 0 | 37 | 38 | 25 | 0 | 0 | 7.8 | 5.6 |
| LED | 14 | 45 | 27 | 14 | 0 | 0 | 5.3 | 6.2 |
| Liquid crystal | 13 | 25 | 50 | 12 | 0 | 0 | 6.4 | 8.3 |
| **MICROPROCESSOR ICs** | | | | | | | | |
| 8-bit | 26 | 26 | 32 | 11 | 5 | 0 | 6.1 | 6.4 |
| 16-bit | 19 | 19 | 50 | 6 | 6 | 0 | 6.9 | 11.3 |
| **FUNCTION PACKAGES** | | | | | | | | |
| Amplifier | 18 | 9 | 46 | 27 | 0 | 0 | 8.2 | 6.2 |
| Converter, analog to digital | 7 | 29 | 43 | 21 | 0 | 0 | 7.4 | 7.2 |
| Converter, digital to analog | 9 | 18 | 46 | 27 | 0 | 0 | 8.4 | 8.6 |
| **LINE FILTERS** | 18 | 9 | 55 | 18 | 0 | 0 | 7.5 | 7.4 |
| **CAPACITORS** | | | | | | | | |
| Ceramic | 34 | 33 | 26 | 7 | 0 | 0 | 3.9 | 3.9 |
| Ceramic monolithic | 25 | 42 | 25 | 8 | 0 | 0 | 4.1 | 4.4 |
| Ceramic disc | 35 | 22 | 30 | 13 | 0 | 0 | 4.9 | 4.2 |
| Film | 14 | 33 | 43 | 10 | 0 | 0 | 5.7 | 6.3 |
| Electrolytic | 21 | 21 | 42 | 12 | 4 | 0 | 6.7 | 6.0 |
| Tantalum | 26 | 26 | 33 | 11 | 4 | 0 | 6.0 | 6.2 |
| **INDUCTORS** | 18 | 23 | 47 | 12 | 0 | 0 | 6.1 | 6.3 |

Source: *Electronics Purchasing* magazine's electronics business survey

# EDN REPRINTS

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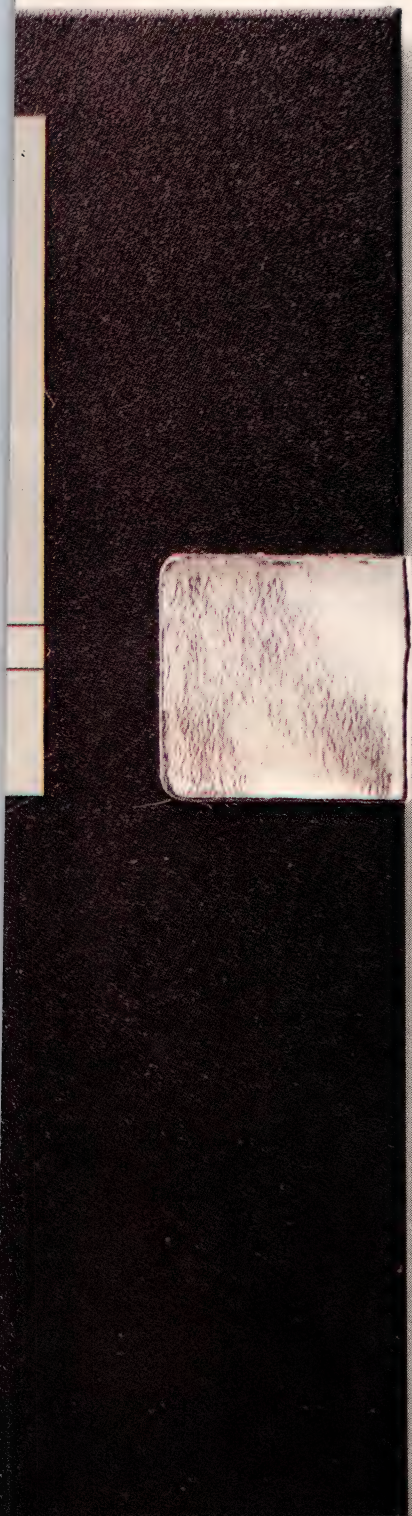

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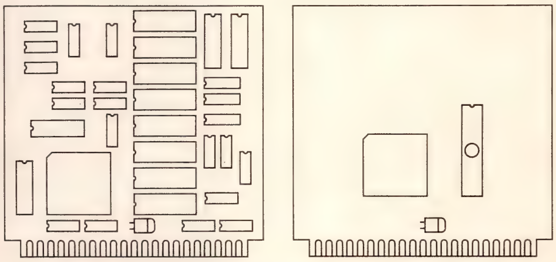

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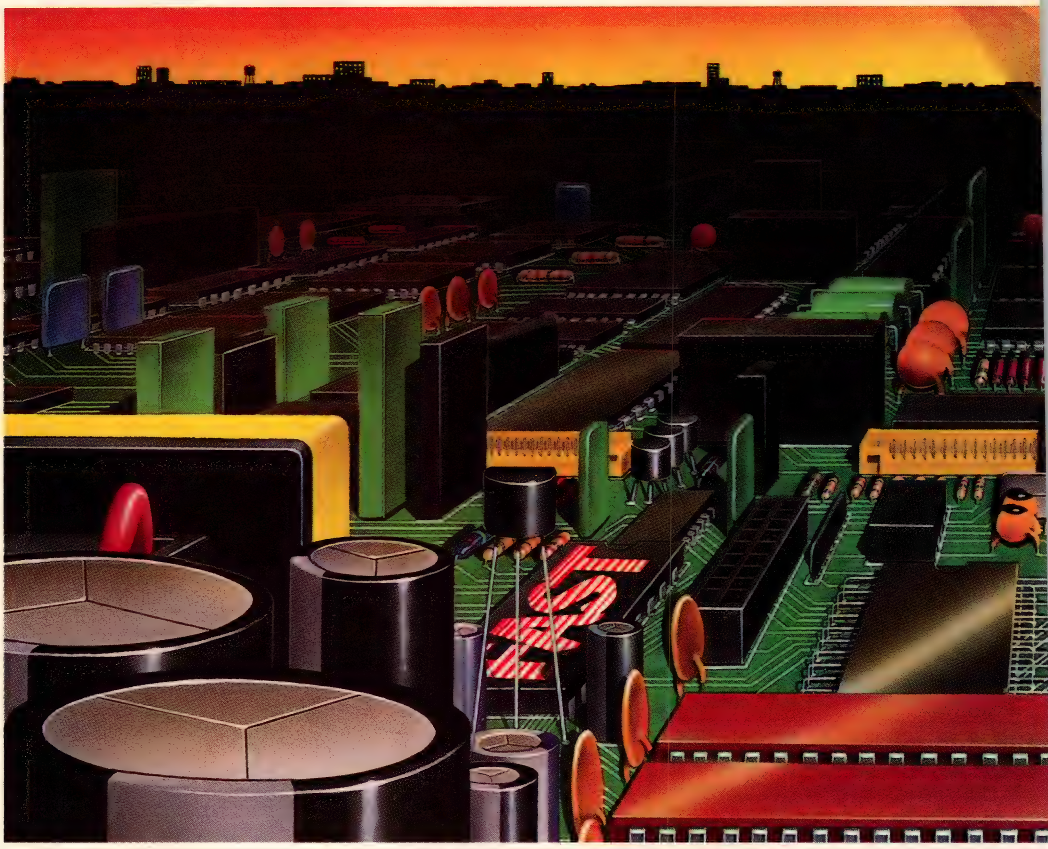

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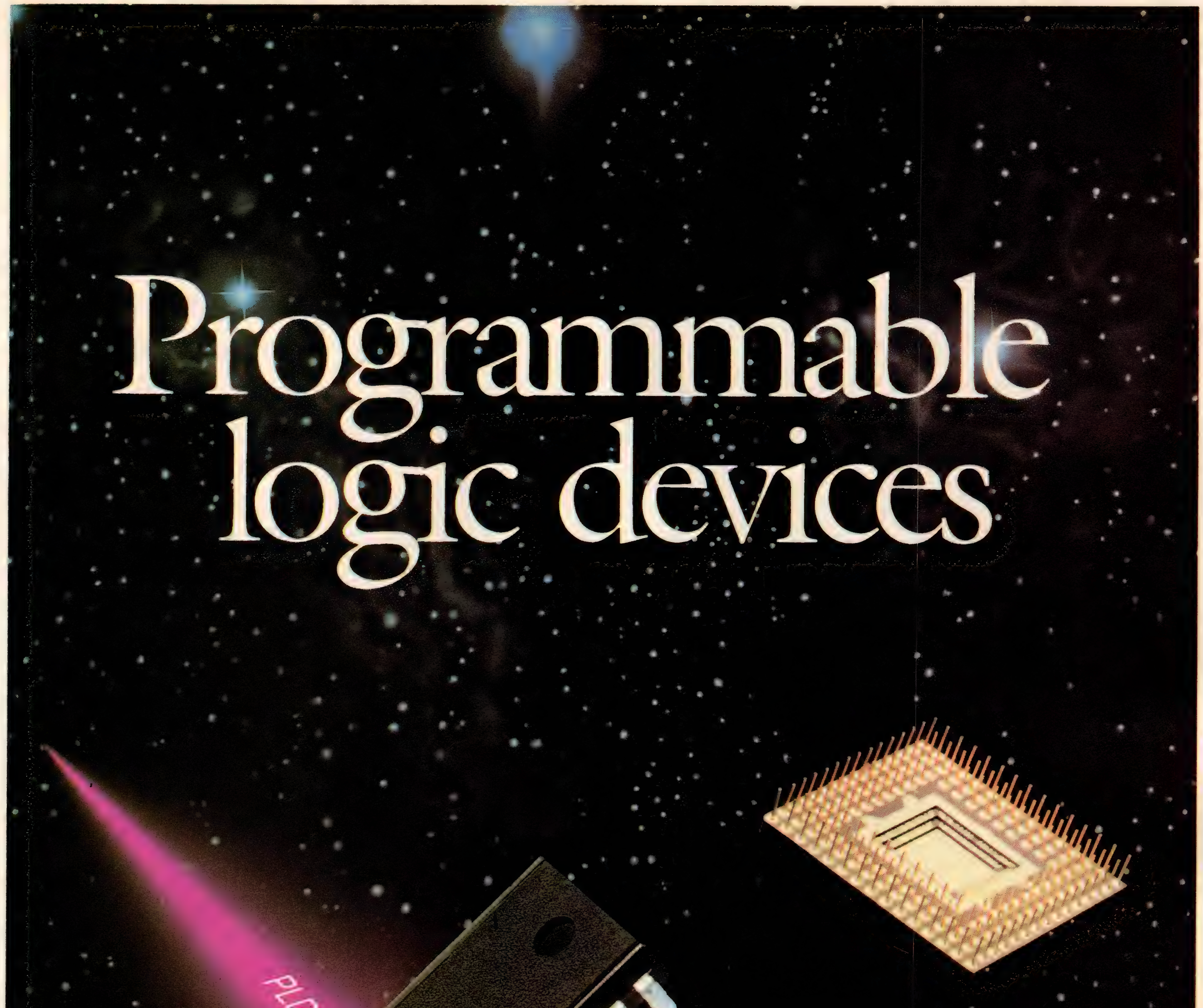



***Today's programmable logic devices*** *offer a spectrum of design benefits. (Photo courtesy Signetics)*

Advances in programmable logic devices' architectures are making PLDs suitable for a plethora of applications. The devices now find use in state machines and other highly sequential circuits. In the past two years, bipolar PLD operating speeds have doubled, and emerging CMOS PLDs offer four times the circuitry per chip that the older bipolar versions offered. CMOS PLDs also offer lower operating currents, erasability and reprogrammability, and testability that promises close to a 100% yield of working parts.

*From its humble origins, the programmable logic device has evolved into a complex part with the ability to implement sequential and combinatorial circuits. CMOS technology lets you reprogram PLDs and reduce system power consumption; bipolar PLDs can help increase system speed.*

David Smith, *Associate Editor*

To evaluate the design potential of PLDs, you must understand their architectural aberrations from the traditional PLA circuit (see **box,** "The basics of PLD architecture"). Each aberration enables the device to implement certain types of circuits that the original couldn't manage. An understanding of how the benefits of CMOS PLDs affect your particular system will help you determine whether the higher price of the CMOS parts is worth those benefits. Bipolar PLDs are seeing speed improvements that render them useful in higher-speed systems traditionally served by SSI and MSI chips. But when evaluating these chips, don't consider only functional specs. You should also consider factors like programming yield, software support, testability, and reprogrammablility and how they influence the design and manufacturing process.

Most new PLD architectures expand on the basic AND-OR structure of the original PLDs. They offer programmable output cells that let you set the polarity of the output signal; the cells often include an output-enable feature as well. These cells can also include a register and several feedback lines, in which case the cells are called macrocells. Some macrocells, like those in Altera's devices, also include part of the logic arrays. The extent to which they expand upon or deviate from the basic PLA architecture is the most distinguishing characteristic of any PLD.

Deviations from established PLD architectures vary from the barely noticeable to the dramatic. The CMOS PLDs from Sprague Solid State are an example of the former. They're identical in function to Monolithic Memories' bipolar PAL devices, and you can use the Sprague PLDs as direct replacements for PAL devices. Unlike most older devices, however, the Sprague devices include a security bit that you can set to keep a competitor from reading out your design's programming pattern. Most new PLDs include this security bit.

A simple variation on the PAL theme comes from Panatech Semiconductor. The company is the American arm of Ricoh (Osaka, Japan), the only Japanese company presently involved in PLDs. Panatech's CMOS devices contain twice as many product terms per output as their PAL counterparts. The extra product terms allow you to implement more complex algorithms, including XOR instead of OR summing logic. In other functional respects they are identical to PAL devices.

Other companies are offering PAL-compatible devices that include more circuitry than do the standard parts. VLSI Technology offers CMOS PAL replacements with what it calls an X-pander cell, which connects the product terms of two adjacent output cells, doubling the number of product terms available to each output. In addition, the cell can perform an OR or an XOR function on the product terms available to it. Atmel, a year-old company offering EPROMs and electrically erasable ROMs, will use a 1.25-μm CMOS technology to create a 20-pin PLD. Scheduled for release by the end of the second quarter, the company's V750 will include twice the number of sum terms, registers, and feedback lines that are normally associated with 20-pin devices.

Another new architecture implements a PAL superset in a chip that you can program to operate like a PAL device. Lattice Semiconductor offers such an architecture in its GAL devices, for example. The GAL (generic array logic) devices, for which VLSI Technology is an alternate source, can replace most 20- and 24-pin PAL devices. For example, the GAL 16V8 20-pin

PLD can replace any of the following PAL Series chips: 10X8, 12X6, 14X4, 16X2, 16X8, 16X6, and 16X4 (where X stands for L, H, P, or RP). By including the options found in *all* of those devices, the 16V8 can offer some combinations of options not available in any one PAL device. Furthermore, the availability of all the options in one device allows you to stock only one chip type instead of as many as 21 different types.

The GAL devices also feature reprogrammability and lower power consumption than the PAL devices do. The GAL advantages come at a higher cost, however; one with a 25-nsec propagation delay (the time it takes a change in state at a PLD's inputs to reach its outputs) costs $8.80 in a plastic DIP; the devices it can replace cost from $3 to $7.

Another PLD that can replace a variety of 24-pin PAL devices is Cypress Semiconductor's EPROM-based 24-pin PLD C 20G10. It specs a 25-nsec propagation delay and consumes 55 mA, which is lower than the GAL 20V8 24-pin PLD's 90 mA and the 180-mA stand-

## The basics of PLD architecture

The first programmable-logic devices implemented Boolean sum-of-products logic to replace the growing number of SSI and MSI chips proliferating on pc boards. The early PLDs usually included the coding, decoding, multiplexing, and demultiplexing logic needed to allow LSI devices to communicate with each other. Boolean algebra was chosen as the basis for PLD logic because it was taught in most engineering schools.

A PLD uses a programmable logic array (PLA) whose exact function you can program, either by melting fuses or by loading memory elements. A PLA (**Fig A**) can generate any possible sum of products for a particular set of inputs. When you program the device, you in effect select the sums of products that you need.

The first PLDs, Signetics's field-programmable logic arrays (FPLAs), contained a PLA in which all product terms and sums were fuse selectable. Although these parts were flexible, they were too complicated for many designers, who were just getting used to designing with SSI and MSI chips.

### Reduced size and delay

With its PAL devices, Monolithic Memories simplified the PLA by assigning product terms to specific outputs (**Fig B**). Fixing the OR array reduces the PAL IC's size by reducing the number of programming elements, and it lowers the propa-

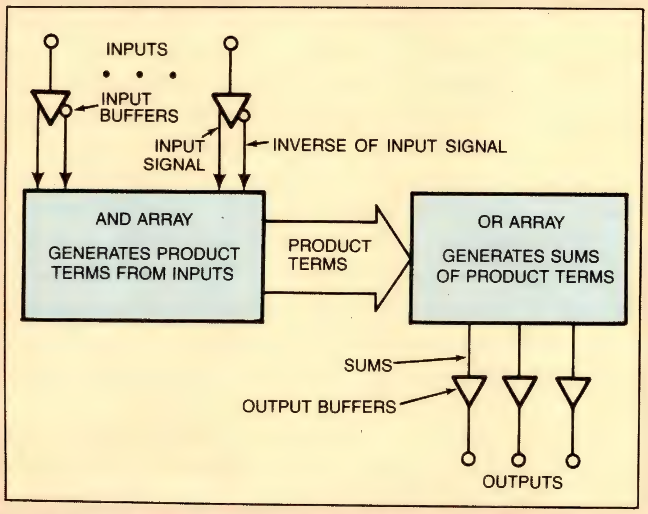



***Fig A—The PLA is the basis for most PLDs.*** *An FPLA includes fuses or memory elements in the AND and OR arrays. To create the logical function you want, you melt fuses or load memory elements into these arrays.*

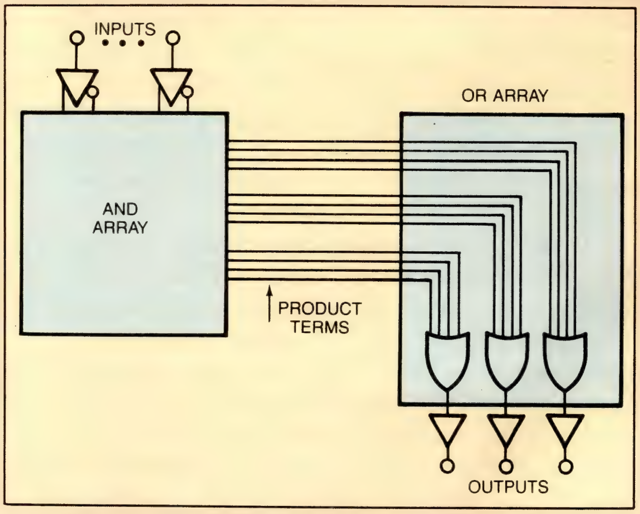



***Fig B—A fixed-OR array in the architecture*** *of Monolithic Memories' PAL devices improves upon the PLA by reducing the die size, creating a faster device, and applying software design tools to the PLD design process.*

*Advances in architecture expand the range of PLD applications from simple coding circuits to state machines and other sequential circuits.*

ard for 24-pin bipolar PLDs. Prices for the PLD C 20G10 start at $6.75.

Another type of architecture, introduced this spring, combines both AND and OR logic arrays into one array, a technique called folding. Feedback lines from the output of the array attach to the inputs, permitting implementation of multilevel logic. For example, inputs to the arrays can form product terms that can attach to the feedback lines. The product terms themselves become inputs to the array, allowing you to sum those terms for a sum-of-products logic circuit. You can assign any term to a feedback line, and you can create a design that effects product-term sharing.

The Erasic (electrically reprogrammable application-specific IC) from Exel Microelectronics is the first commercially available PLD to employ the folded-logic-array architecture. The company refers to the product's architecture as a configurable logic array, which consists of one programmable array with feedback lines **(Fig 1)**. Because the number of times you route signals

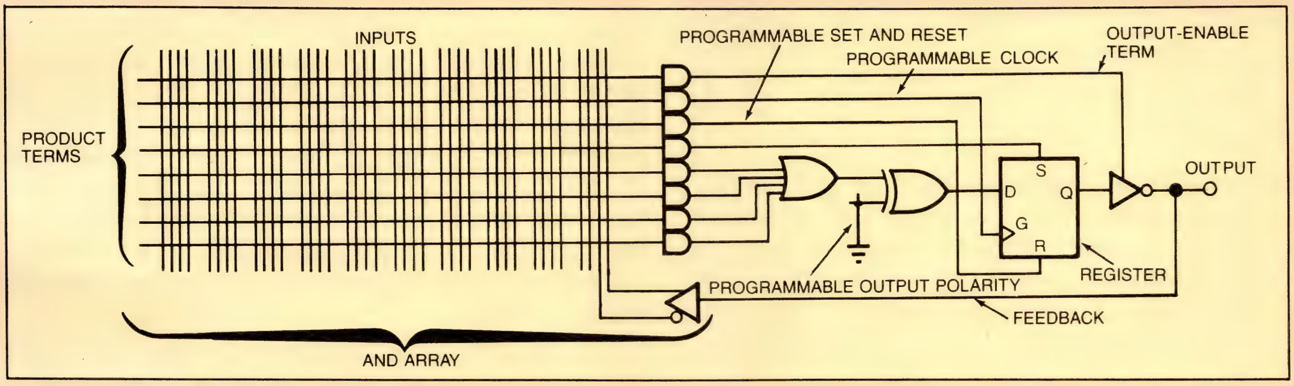



***Fig C—Modern PLDs include programmable features*** *not found in the original PLDs. These features control the operation of internal registers, control the output buffers, and introduce internal feedback.*

gation delay through the PLD. However, the practice limits the number of product terms in each sum and doesn't allow any product term to go to more than one sum (ie, it doesn't allow product sharing).

Most important, the simplification of architecture allowed Monolithic Memories to introduce software—Palasm—that facilitates the design process. Palasm accepts your Boolean equations and generates the programming pattern that implements the equations. With PAL devices and Palasm, you don't need to understand the circuit within the PLD to use the device.

As they've evolved, PLDs have incorporated other features that allow the devices to effect circuitry more complex than that which can be represented by straight Boolean algebra. **Fig C** shows modern PLD architecture with some of these features:

- PLDs contain registers that store the sums of products. You use the registers to design synchronous circuits and sequential logic, such as a state machine.
- You can program PLDs that have programmable output polarity for either active-high or active-low output signals.
- Feedback from an output to the AND array allows you to use that output as a bidirectional I/O line. Alternatively, you can drive the contents of the register back into the AND array, creating a state machine.
- Some PLDs contain product terms that enable the output buffers. Consequently, your design can enable the buffers individually and asynchronously.
- Other product terms may connect to the clock input of internal registers (a programmable clock), allowing your logic to clock individual registers.
- Product terms can drive the set and reset lines of internal registers.

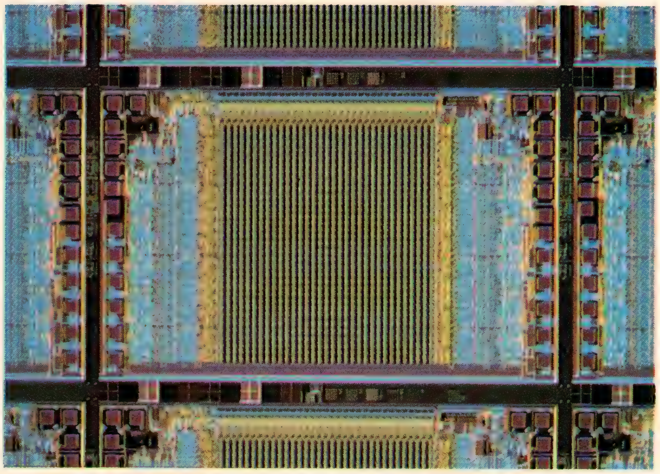


*__Fig 1—One logic array with feedback__ can implement multiple levels of logic. The first PLD with this folded-array architecture, the Erasic from Exel Microelectronics, contains 32 feedback paths and is electrically erasable.*

back into the array is arbitrary (as many as 32 product terms can feed back into the array), you implement nested logic more efficiently than you can using an AND-OR architecture. You can also implement a single level of logic that, by bypassing a second logic plane, yields a shorter propagation delay than would a 2-level logic device.

The CMOS Erasic consumes 35 mA max and specs a 35-nsec propagation delay for one level of logic. It's pin compatible with many 24-pin PAL devices. The device contains feedback lines from its output registers to its logic array, so you can use it to create state machines with buried registers. Like many CMOS ICs, it doesn't drive as large a load as bipolar devices can; it sinks and sources only 4 mA, so it can't drive more than two TTL loads.

Signetics is developing a folded-logic-plane architecture for its bipolar parts. Devices with that architecture will contain buried registers and a flexible interconnect structure. The parts could implement state machines running at 80 to 100 MHz, according to the company. The first ones won't have registers, however, but will offer only a 4-nsec propagation delay through the logic plane.

Not all PLD vendors see the folded-logic array as the best architecture for PLDs. Altera's PLDs group logic circuitry, registers, feedback lines, and I/O-control circuitry into macrocells. The macrocells connect to local and global buses that distribute input and feedback signal lines. In addition, these devices have features not commonly found in PAL devices: synchronous and asynchronous clocking, buried registers, variable product-term distribution, and a security bit. Altera offers a family of these devices ranging in complexity from about 300 to 1800 equivalent 2-input gates.

Intel offers devices identical to the 300-, 600-, 900-, and 1200-gate Altera devices. Altera exchanged the device designs for the Intel EPROM technology from which the devices are made. Intel plans to introduce a zero-standby-power version of the 300-gate device that will also deliver a 25-nsec propagation delay and 25-mA current consumption at 10 MHz (a typical PAL device specs a 25-nsec delay and 180-mA power consumption).

Although most complex PLDs are CMOS devices, bipolar PLDs are clearly getting more complex as well. An early example, the 22V10 from Advanced Micro Devices, brought programmable-output macrocells to 24-pin PLDs. The 22V10 can replace a variety of 24-pin PAL devices. The usefulness of this design is not lost on makers of CMOS parts; Cypress offers CMOS versions of the 22V10, and Texas Instruments and Lattice Semiconductor will have CMOS versions by the end of the year. The CMOS ICs consume as much as 50% less power than their bipolar counterparts, and they are reprogrammable.

AMD continues its expansion of bipolar-PLD architecture with its AmPAL23S8 (**Fig 2**). The most noteworthy features of the device are six buried registers. These registers have an average of eight product-term inputs, which in effect add another 48 product terms to a 20-pin PAL-like architecture. These buried registers allow you to build sequential circuits like state machines without using any output pins. By not routing feedback lines from the output registers through output buffers, the buried registers can also clock at higher frequencies than registers in output macrocells.

The AmPAL23S8 offers other features not found on most bipolar PLDs. You can set the polarity of each output separately, and you can program each output buffer so that it's enabled by its own product term. The eight outputs consist of four output registers and four output macrocells that offer a choice of registered or unregistered operation and a choice of several feedback modes. One product term can operate as a synchronous preset, and another can operate as an asynchronous reset. Both product terms operate on all registers in the device.

Large bipolar PLDs do not have an enviable history. MMI attempted to realize large architectures in bipolar technology via its MegaPAL devices. They maintain the PAL AND-OR structure but offer as many as 32 inputs,

*One new PLD architecture includes a superset of all PALs in one device that you can program to operate like a PAL.*

32 outputs, and 255 product terms. This fixed-PAL structure makes it difficult to apply these devices, and their 640-mA max operating current renders them too power hungry for most designs. The AND-OR structure that works well for collecting several MSI and SSI functions doesn't seem to implement larger circuits nearly as well. Nevertheless, the manufacturer claims that the devices' popularity is slowly increasing.

Improvements in the FPLA architecture are appearing as well, although they're less dramatic than the improvements in PAL architectures. For example, Signetics's PLS167 and PLS168 have a preset option that allows you to initialize output registers. The devices also include a complement array that generates the negation of any product term you choose and feeds it back into the AND array. You can then use the term in subsequent product terms.

Only one vendor, Xilinx, has abandoned the PLA-based PLD design altogether in favor of an architecture more like that of a gate array. Xilinx's PLD, the XC 2064, comprises 64 individual blocks of logic in a sea of interconnects. Both the blocks and the interconnects are programmable. Because the circuits you build don't conform to a PLA-like structure, you have more freedom in using registers than you do in the PLA-based devices.

You use the logic in a logic block in a way similar to the manner in which you would define the function of cells in a gate array. Each logic block (**Fig 3**) contains a 4-input logic cell that can implement logic functions. The blocks also contain a register and feedback lines. The XC 2064 can implement as many as 1500 equivalent gates of logic, so you can use it instead of a small gate array, in place of 15 to 75 SSI and MSI ICs, or as substitutes for as many as four PAL devices, according to the vendor.

Most of the companies new to the PLD market are concentrating on CMOS devices, because the technology can yield PLDs that are amenable to more circuit designs than are bipolar PAL devices. The principal advantage of CMOS is that, by virtue of its simpler layout and lower power consumption per unit of silicon area, it can create much more dense and complex circuitry. Also, any CMOS part should have better supply-voltage tolerance and noise margins than corresponding bipolar parts. CMOS vendors list other bene-

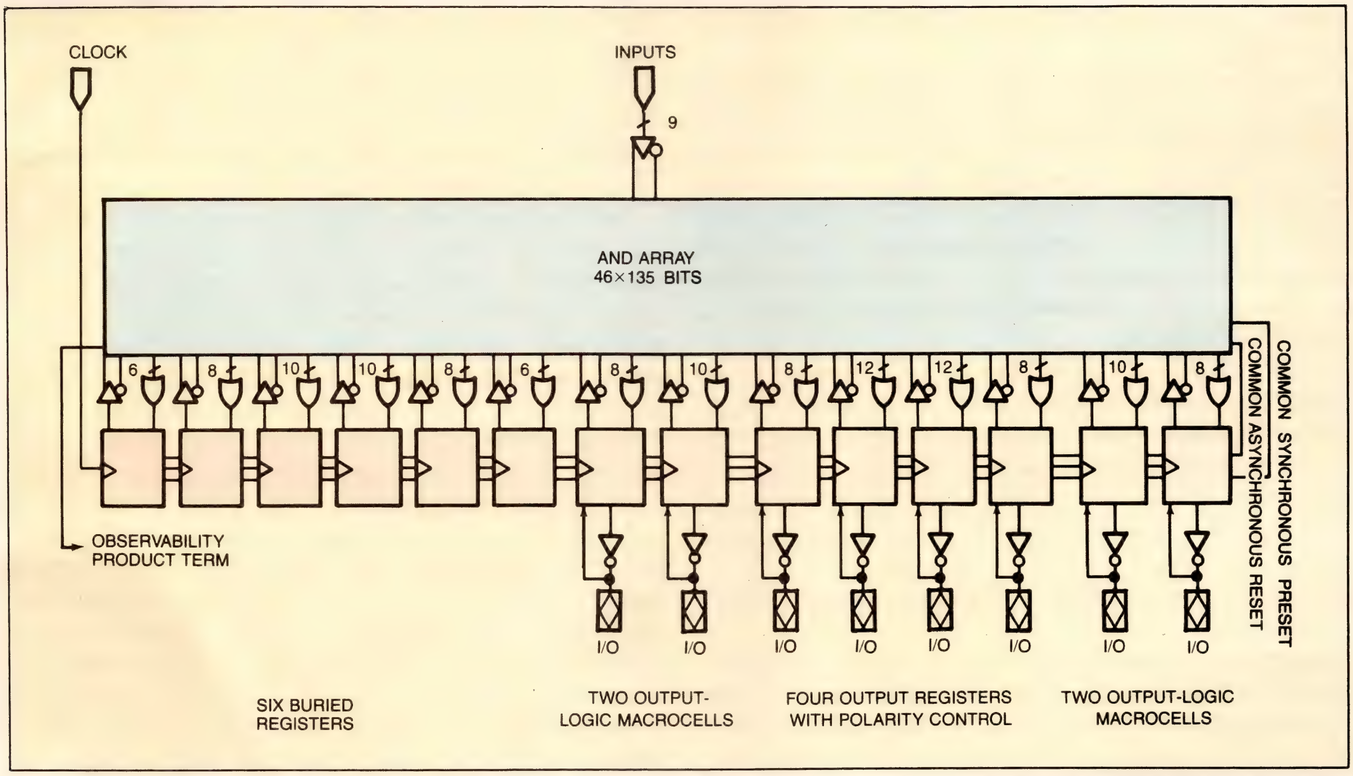



***Fig 2—Buried registers build fast state machines*** *in the AmPAL23S8 from AMD. You can preload the buried registers through the output pins to facilitate testing.*

*A technique called "folding" combines AND and OR logic arrays into one array.*

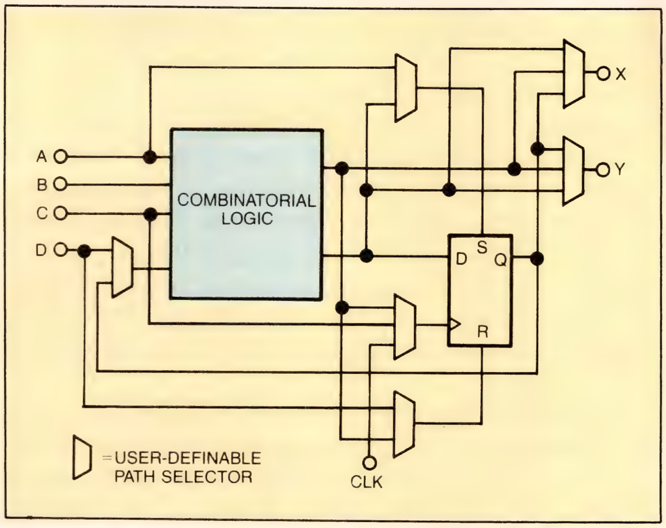



***Fig 3—The placement of programmable logic cells** in a sea of interconnects is the distinguishing feature of the Xilinx XC 2064. The logic cell includes combinatorial logic, a register, and path selectors for configuring the cell.*

fits—lower power consumption in its own right, testability, and erasability—but you should inspect them carefully to determine whether they actually benefit your design.

For example, though CMOS devices generally consume less power than equivalent bipolar devices, at high frequencies they may actually consume the same amount of power, because CMOS power consumption is proportional to operating frequency. Check the power consumption at the frequencies at which you expect your circuit will operate. Quarter- and half-power bipolar devices may consume the same amount of power as some CMOS devices.

AMD offers half- and quarter-power versions of its 18P8. The half-power version specs a 25-nsec propagation delay and 80-mA max operating current. The quarter-power version specs a 35-nsec propagation delay but a cool 45-mA max current. Comparable CMOS devices, Lattice Semiconductor's quarter-power GAL16V8 and Cypress Semiconductor's PAL C 16XXL-25, spec a 25-nsec delay and 45-mA current consumption.

Look for the frequency at which the vendor determines maximum power consumption. Maximum power consumption for CMOS devices is often measured at 10 MHz, but if you plan to use the full speed of a 35-nsec CMOS PLD, the device will use more power than it would when operating at its 10-MHz rating. Ask the manufacturer to estimate the power consumption at your frequency requirements.

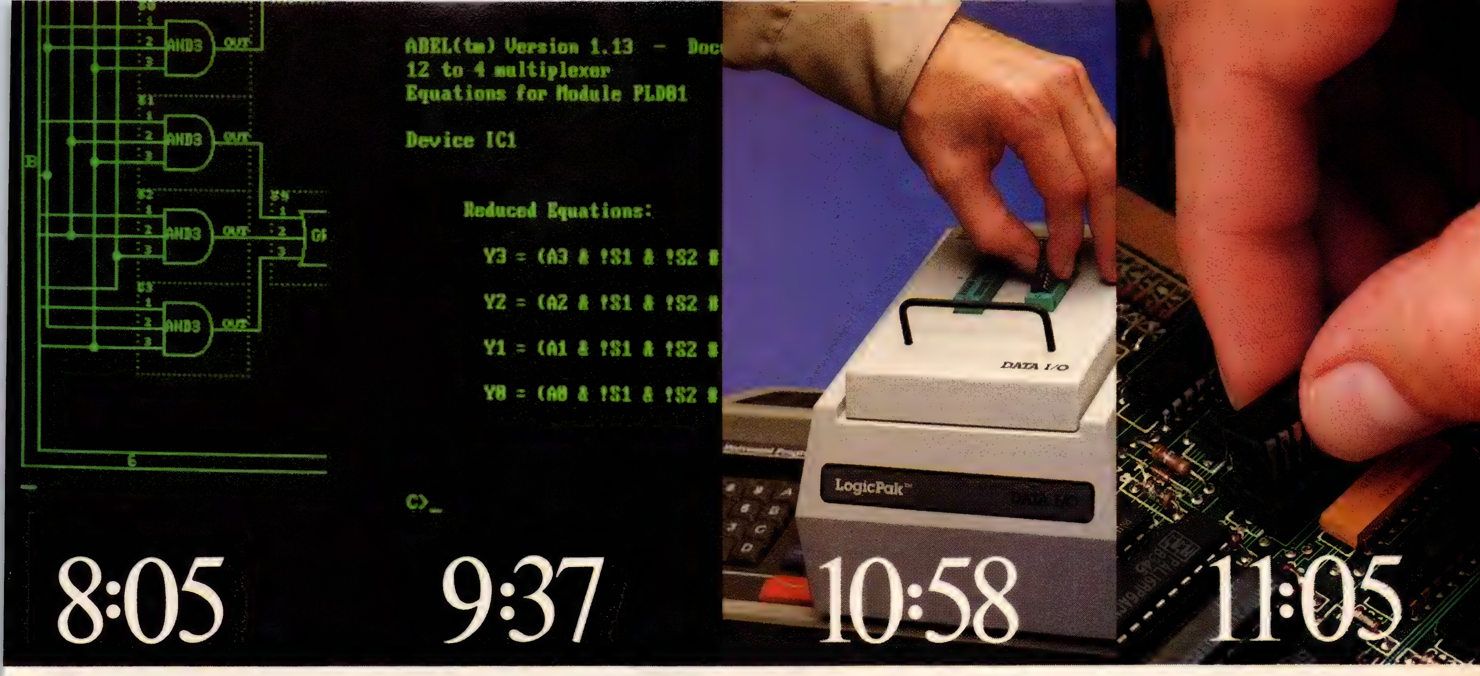
Even in those cases where the CMOS part consumes roughly the same power as a bipolar part during operation, the CMOS part will still save you power when it's idle. Unlike bipolar devices, which have a significant quiescent current, CMOS devices fall into a quiescent mode that consumes much less power than does the active state. Zero-power CMOS PLDs can consume microwatts when idle, but it takes some time for most PLDs to enter a quiescent mode. If that power-down time is longer than the time your circuit is typically idle, then the PLD won't achieve quiescent operation very often.

CMOS devices like Altera's can drop into a quiescent state immediately once the outputs stop switching. Others, like the Xilinx part, contain an inactive power-down pin that you must assert to put the device in that mode. The Xilinx part consumes only 50 nA in quiescent mode.

Harris offers CMOS replacements for bipolar PAL devices and chip-select decoders. The relatively slow CMOS PAL replacements (typical propagation delay is 125 nsec) spec 6-mA/MHz power consumption and a 150-μA standby current, so they are appropriate for circuits with slow and infrequently changing signals. The Harris chip-select decoders can replace two to seven ICs in memory and I/O chip decoding circuits. They spec a 60-nsec propagation delay.

CMOS is also used to create hard-wired versions of PAL devices. Vendors of the hard-wired versions customize their parts through use of a metal mask during processing. The devices are therefore fixed, not programmable. Monolithic Memories' HAL (hard-wired array logic) devices and VLSI Technology's mask-programmable logic arrays use less power than PAL devices, aren't quite as fast, and might not sink as much current, but in large quantities they will cost much less than programmable parts.

After noting the new architectures and the emergence of CMOS parts, you'll observe that today's PLDs have become faster as well, and it's little wonder that they have. Performance is the most important parameter for PLDs; many PLD vendors describe their customers as "speed freaks" who are always crying for faster devices than are available at any given time. Bipolar ECL PLDs now offer propagation delays as short as 6 nsec. TI and Fairchild plan to introduce 3-nsec devices by the end of the year. Because PLDs

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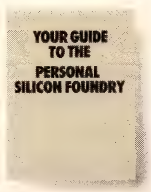


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CIRCLE NO 82

*By using devices with buried registers, you can implement sequential circuits like state machines without using any output pins.*

replace the equivalent of two or three levels of logic, the present ECL versions are roughly equivalent in performance to discrete ECL parts (which typically spec a propagation delay of 2 nsec).

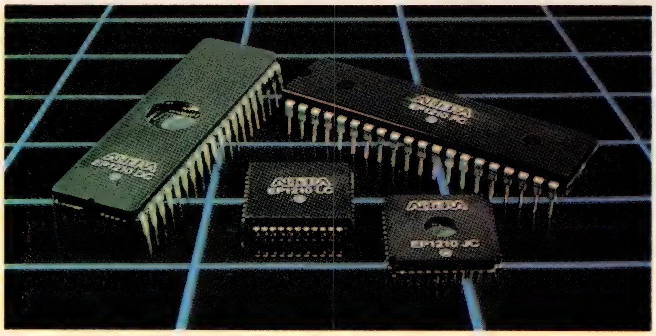
TTL PLDs are also getting faster and are superior to CMOS parts in speed. For example, Monolithic Memories' PAL 24B Series and 20B Series devices, TI's Impact PAL devices, and Fairchild's 16P8B device furnish a propagation delay of only 15 nsec. These companies all plan to introduce 10-nsec TTL devices by the end of the year. The fastest CMOS devices feature a propagation delay of 25 nsec. The high-speed bipolar PLDs can require as much as 210 mA max power-supply current but are otherwise identical to regular PAL devices.

Typical TTL bipolar parts, with propagation delays of approximately 25 nsec, compete directly with CMOS parts. As noted, the CMOS parts consume as little as 50% of the power of bipolar equivalents, but you pay a price premium to use them. Remember also that half-power TTL devices can consume as little as 90 mA, and quarter-power TTL parts as little as 45 mA. Though these lower-power PLDs are slower than their full-power counterparts, the lower-power versions may consume roughly the same amount of power as equally fast CMOS parts.

By integrating more logic, CMOS parts could compensate for their relative slowness and achieve competitive system-throughput levels. With more feedback lines allowing more complex state machines, your system design could be as fast with one CMOS part as it would be with two or more PAL devices or a PAL device and other discrete logic. However, CMOS parts may not be able to drive the high currents that bipolar parts can, so you must consider the load that your system places on your PLD.

The complexity you can realize from the simple layout of CMOS devices does make timing analysis of the parts more difficult. The multilevel devices can theoretically include any level of nesting (up to the number of feedback terms into the logic array). Ideally, your design software should verify the dynamic performance of your part, but not all PLD design tools can simulate the newer, more complex PLDs.

Higher complexity—in any type of device—exacerbates problems related to testing. Functional testing is not always necessary with PAL designs, but feedback terms will introduce a variety of dynamic signal paths that you may have to verify. Also, on-chip registers



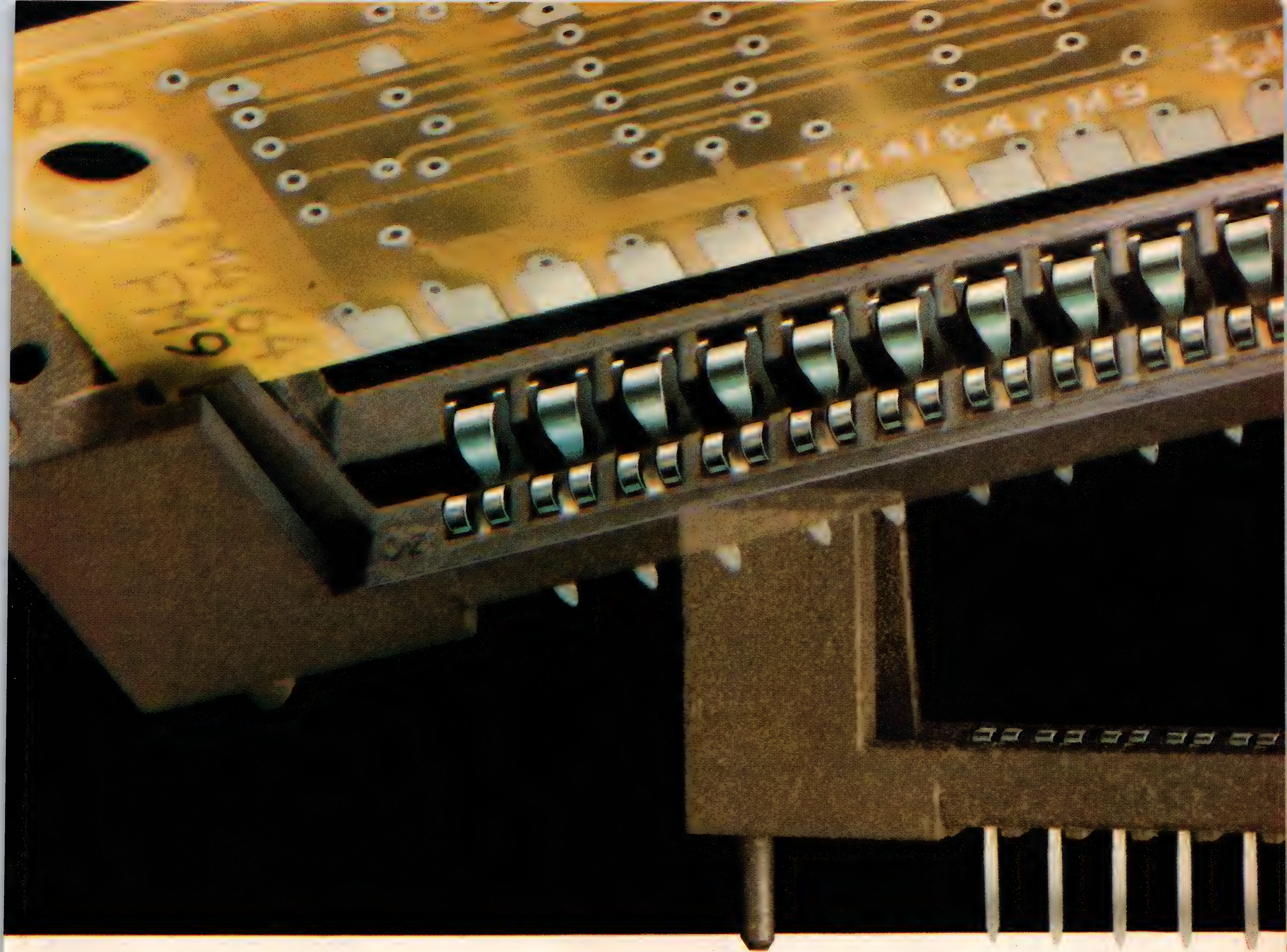
***Packages with windows are necessary** to erase CMOS PLDs that are built with EPROM technology. Vendors of these devices offer windowed packages for prototype development and lower-cost plastic packages for production systems.*

require a preset or preload function to put them into a known state. Fortunately, most PLDs with registers include such functions.

From the manufacturer's point of view, CMOS's biggest asset is its testability. CMOS PLDs usually use reprogrammable technologies based on EPROM or EEPROM cells. The vendor can set the cells to test the device and then erase them before shipping. The erasability of EPROM and EEPROM cells makes the parts good candidates for prototype development; you can design incrementally and fix minor bugs without rewiring your boards. Bipolar fuses, on the other hand, cannot be restored once they are blown, so vendors can't test the fuse array and circuitry immediately adjacent to it.

Lattice Semiconductor encourages its customers to forego incoming and dynamic testing because the company completely tests its electrically erasable CMOS PLDs (although it will supply Sentry test vectors if asked). The savings gained by eliminating some device testing become significant at higher production volumes, in the form of reduced handling, testing, and inventory costs. In addition, the costs of sorting and returning devices are eliminated.

Still, most manufacturers of bipolar parts say that they can achieve a greater than 99% postprogramming functional yield (PPFY), so if the 1% fallout is acceptable, testability may not even be an important factor in your evaluation of PLDs. (The PPFY denotes the percentage of functionally good parts after the entire lot of PLDs has been programmed.) Because the design and testing of fuse-programmable PLDs is a mature art, vendors of bipolar devices declare that they can test virtually all functional circuitry without program-







CIRCLE NO 68

*One vendor has abandoned the PLA-based PLD design altogether in favor of an architecture that's more like that of a gate array than a PLA.*

ming the entire logic array. According to Mitch Richman, product marketing manager at AMD, internal testing circuitry allows the company to deliver parts that achieve a PPFY of greater than 99.9%.

The 99% figure that vendors of bipolar PLDs cite is usually mentioned in reference to the simpler PAL devices. More complex architectures, with buried feedback terms and registers, require fuses within the macrocells to effect these features. As noted, these fuses can't be blown for testing, so the testing problem for complex fuse-programmable devices is more intractable than it is for simpler architectures. Therefore, don't expect the PPFY figure to be as high for the big bipolar PLDs.

One manufacturer of bipolar PLDs, AMD, mitigates the testing problem by making its buried registers in the AmPAL23S8 accessible to the output pins. One product term enables a preset mode for the registers, allowing you to load the registers through output pins that are otherwise connected to output macrocells and registers. This arrangement allows AMD (and the user) to set the buried registers into a known state to begin testing.

The need to develop tests for PLDs has come to the attention of vendors of PLD design systems and of test systems. They are introducing software to assist you in creating tests for your PLDs. These tests work from a description of the device and your programming pattern to develop test vectors. In addition to developing test vectors, software from Teradyne (Boston, MA) runs a fault simulation, a necessary step for PLDs that incorporate thousand-gate complexities.

## PLD design software: straining to keep pace

Design software isolates you from PLD architecture, allowing you to design more naturally (as you would with discrete ICs). Just as Palasm translates Boolean algebra into PAL fuse maps, more advanced design software translates your state-machine designs and truth tables into programs for more complex PLDs.

The proliferation of new PLD architectures, however, is making it difficult for vendors of PLD design software to provide design support for all types of PLDs. When you consider using a complex PLD, first determine which design tools can create the programming patterns for it.

### Relieve the tedium

You can design most PLDs by hand. To do so, you need to understand how a PLD's circuitry implements logic functions, and then you fill out a program table for that PLD. Program tables contain rows and columns of boxes that represent locations of programming elements on the PLD. Creating a PLD design this way is a long and tedious process.

Basic design tools such as MMI's Palasm and Signetics' Amaze automate the construction of a fuse map. You enter Boolean and state-machine equations into the software, and the software generates a file with the programming code. These tools also include functional simulators that let you verify the function of your PLD design. Like most PLD design tools, Palasm and Amaze can run on personal computers.

Not all designers use Boolean logic equations, especially for designs containing hundreds or thousands of gates, and these alternative design approaches require more advanced design tools. Third-party companies (not the PLD vendor or its customer) are now offering such design tools. Abel from Data I/O (Redmond, WA) and Cupl from Assisted Technology (San Jose, CA) are examples of these tools; you can use truth tables, state diagrams, and schematic capture in addition to Boolean equations. Another benefit of using third-party tools is that they support a wider range of PLDs than tools from a PLD vendor.

### Keeping up with architectures

The expansion of PLD architectures has put a strain on the PLD software that was developed for PAL and FPLA architectures. The existence of this software guarantees the utilization of those devices for some years until more flexible software becomes widely distributed. In the meantime, vendors of new architectures generally offer their own design environments. These more recent design tools are usually more powerful, but they are also exclusive to a particular family or vendor.

Because its devices have an architecture that's significantly different from those of PALs and FPLAs, Altera offers a PLD-de-

If you have narrowed your PLD candidates to CMOS parts, differences between EPROM-based PLDs and electrically erasable (EE) PLDs may affect your choice of device. Vendors of EPROM-based parts must place the devices under a lamp to erase programming patterns when reprogramming the parts for more tests. EE PLDs can be erased in the test equipment. Still, EPROM-based vendors claim to provide as high a level of testing as EE PLD vendors. For example, Cypress Semiconductor borrows a technique from bipolar vendors to test its PLDs. One portion of a part's logic array is programmed at the factory for functional and ac testing; this phantom array remains programmed so you can test the part upon delivery.

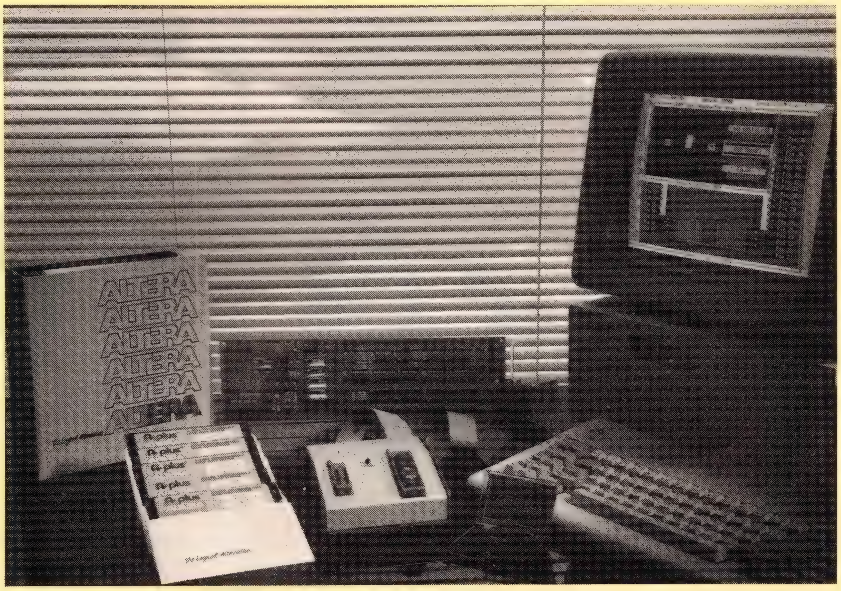
The basic prices of EE PLDs are higher than those of EPROM-based PLDs because the process technology is more difficult to control. In addition, the programming-cell size of EE PLDs is larger by two to three times than EPROM cells (estimates depend on the technology used, and few companies release exact figures). As a result, EE PLDs tend to cost more. Lattice Semiconductor's 20-pin EE PLD, the GAL 16V8, costs $8.80 (1000), while an EPROM-based device of similar complexity, Altera's EP310, costs $6 in a plastic DIP. To take advantage of the EP310's reprogrammability, however, you'd order the part in a package with a window at a cost of $10.75.

As PLDs become more complex, which usually means more I/O circuitry and feedback, the percentage of area covered by programming cells will decrease. Consequently, the size advantage of EPROM-based devices will shrink. Because the memory-cell-size advantage

sign package. The A+Plus design package includes design software and programming hardware that consists of a card for your computer and a programming box. When running A+Plus on an IBM PC, you can enter your design as a schematic or a net list, and you can enter Boolean equations and state-machine diagrams. Intel, which uses Altera's EPLD designs, offers a similar package.

Xilinx's PLDs differ radically from other PLDs, so the company offers the Xact development system, which runs on the IBM PC. Xact presents you with a graphic depiction of the chip's architecture. You place the logic function you need on one logic cell in the architecture and identify connection points; the software then assigns a programming pattern to the logic cell and finds an interconnection path. When you've completed placing your logic functions, the program can functionally simulate your design. Xact also performs timing simulation.

The most unusual feature of Xact is its ability to perform in-circuit emulation. You place an emulation pod, which is connected to the PC, over the XC-2064 PLD on your prototype pc board. You can download designs into the chip through the pod and transfer the state of the chip's registers back into the PC for debugging. As you test your prototype, you can observe the operation of the PLD and download design changes without removing the chip from the board.




***Design software and programming hardware*** *convert your IBM PC into a workstation for designing and programming Altera's PLDs. You can enter your design as a schematic, as Boolean equations, as a truth table, as a state diagram, or as a combination of these forms.*

should decrease and packages with windows will always be considerably more expensive than plastic packages, EE PLDs should eventually become the most cost-effective of the complex CMOS PLDs.

EE cells also offer the designer the capability to reprogram the chip within the circuit design. However, for production runs, the value of reprogrammability is uncertain. Few current applications require hardware that configures itself, although in the words of Alex Goldberger, technical marketing manager at Exel Microelectronics, "Give it [in-situ reprogramming] to designers and they'll figure out a way to use it."

The Xilinx CMOS PLD, with its gate-array-like architecture in which RAM cells control macros, doesn't employ the expensive process of EE PLDs, nor does it feature the window and reprogramming time of EPROMs. It is volatile, however, and it's expensive (prices start at $55). Xilinx designed the part so that it can load its programming pattern from an EPROM by itself, but the added design effort and complexity of that programming-pattern memory must be taken into account when choosing parts.

With the availability of a variety of PLD types, speeds, and power-consumption specs, the devices will find use in a wider variety of applications than you may have thought possible. You can use the smaller PAL devices in faster and faster systems. Usually these parts have been used to create multiplexing and encoding circuits, and they remain ideal for those tasks. ECL PAL devices can replace parts in mainframes and minicomputers. The CMOS devices, with more than a thousand gates, serve in applications for which you might otherwise have considered small (1000-gate) gate arrays.

To review the spectrum of circuits that PLDs can implement, examine the PLD-design handbooks that most PLD vendors offer. These handbooks typically include several application descriptions. For example, AMD's handbook shows PLD designs for a 4-bit registered barrel shifter, an interface between the Z Bus and an 8086 μP, and a Multibus arbiter. (See also the April 17, 1986, issue of EDN, pg 200, for an application of a PLD in a motor-control circuit.) These examples demonstrate that PLDs are much more than mere generators of Boolean logic. **EDN**

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| | EPL14P4A/B | 14-Input, 4-Output AND-OR/XOR Array | 14H4 14L4 14P4 |
| | EPL16P2A/B | 16-Input, 2-Output AND-OR/XOR Array | 16H2 16L2 16P2 16C1 |
| GROUP II | EPL16P8B | 16-Input, 8-Output, Feedback AND-OR/XOR Array | 16H8 16L8 16P8 |
| | EPL16RP8B | 16-Input,8-Output,8-Registered Feedback,AND-OR/XOR Array | 16R8 16RP8 |
| | EPL16RP6B | 16-Input,8-Output,6-Registered Feedback,AND-OR/XOR Array | 16R6 16RP6 |
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*Series 20A 55ns $t_{PD}$ max
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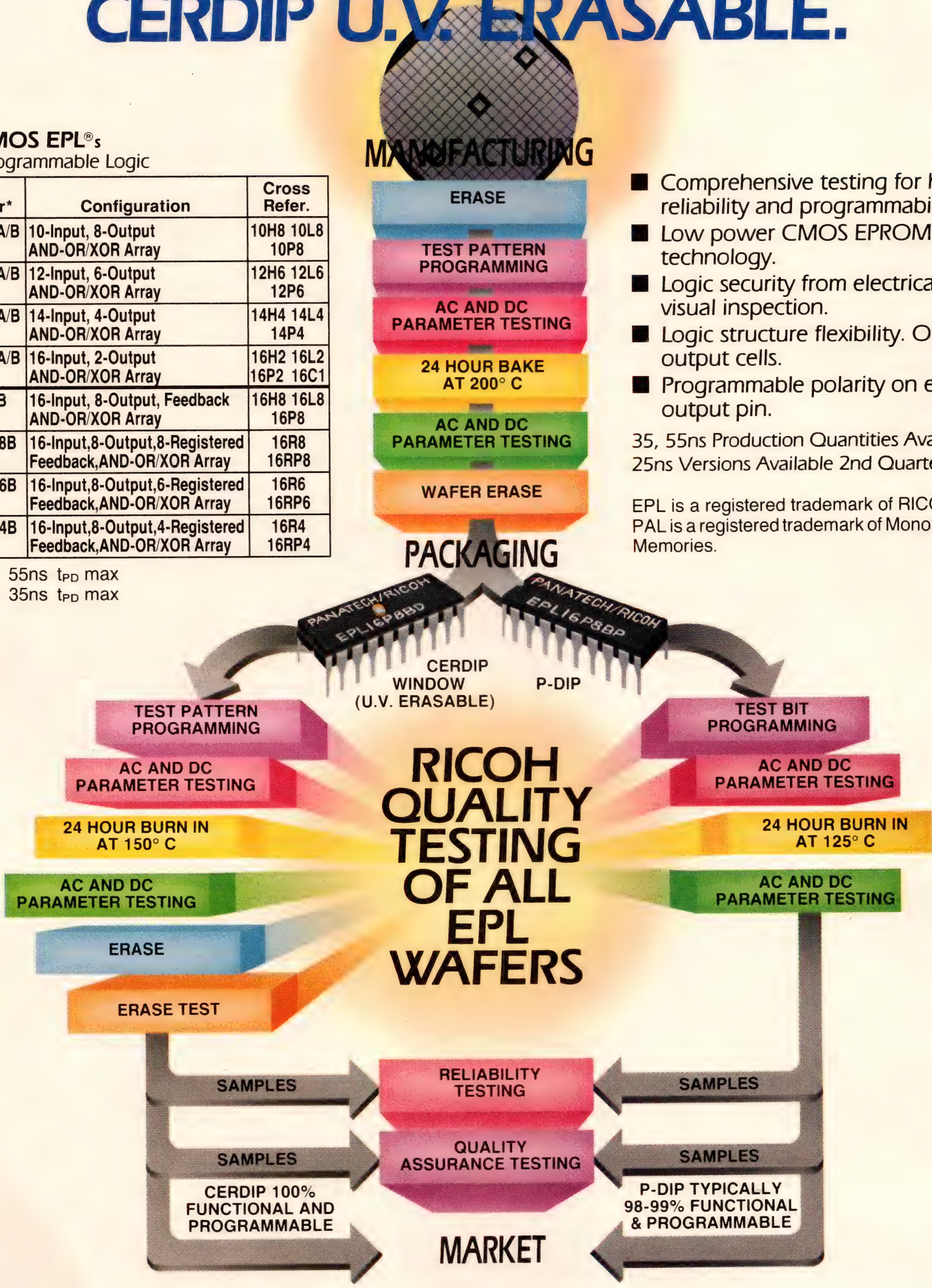


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|---|---|---|---|
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| | 18PB | BIPOLAR | SUPERSET OF COMBINATORIAL 20-PIN PALs |
| | 22V10, 23S8 | BIPOLAR | 24 PINS, OUTPUT MACROS, BURIED REGISTERS (23S8) |
| | 29PL141 | BIPOLAR | PROGRAMMABLE CONTROLLER WITH 64 32-BIT WORDS |
| ALTERA CORP | EP FAMILY | EPROM CMOS | FAMILY OF PLDs WITH CAPACITIES OF 300 TO 1800 EQUIVALENT GATES IN MACROCELL ARCHITECTURE |
| ATMEL CORP | V750 | EPROM CMOS | 22V10-COMPATIBLE PLD WITH TWO SUM TERMS PER OUTPUT |
| CYPRESS SEMICONDUCTOR | PAL C 20 SERIES | EPROM CMOS | STANDARD AND HIGH-PERFORMANCE VERSIONS |
| | PLD C 20G10 | EPROM CMOS | EMULATES 10 24-PIN PALs |
| | PAL C 22V10 | EPROM CMOS | 22V10 COMPATIBLE |
| EXEL MICROELECTRONICS | ERASIC 78C800 | EE CMOS | FOLDED LOGIC ARRAY WITH FEEDBACK |
| FAIRCHILD CAMERA & INSTRUMENT CORP | 93Z459 | BIPOLAR | 28-PIN FPLA |
| | FASTPLA | BIPOLAR | COMPATIBLE WITH FOUR 20-PIN PALs |
| HARRIS CORP | HPL-82CX38, -82X39 | FUSE CMOS | PROGRAMMABLE CHIP-SELECT DECODERS LIKE 74138/139 |
| | HPL-16XXX | FUSE CMOS | 20-PIN-PAL COMPATIBLE |
| INTEL CORP | 5CXXX | EPROM CMOS | FAMILY OF PLDs WITH CAPACITIES OF 300 TO 1200 EQUIVALENT GATES IN MACROCELL ARCHITECTURE |
| LATTICE SEMICONDUCTOR CORP | GAL XXV8 | EE CMOS | SUPERSETS OF 20- AND 24-PIN PALs; FULL-, HALF-, AND QUARTER-POWER VERSIONS |
| MONOLITHIC MEMORIES INC | SERIES 20 PAL/HAL | BIPOLAR | VERY HIGH SPEED, HALF-, QUARTER-POWER VERSIONS |
| | SERIES 24 PAL/HAL | BIPOLAR | VERY HIGH SPEED, HALF-POWER, STANDARD VERSIONS |
| | PAL20RA10, -16RA8 | BIPOLAR | REGISTERED ASYNCHRONOUS 20- AND 24-PIN PALs |
| | PAL6L16A, -8L14A | BIPOLAR | DECODING PLDs WITH ONE (AND) LOGIC ARRAY |
| | MEGAPAL | BIPOLAR | REGISTERED PALs WITH AS MANY AS 64 INPUTS, 32 OUTPUTS |
| | ZHAL | MASKED CMOS | MASK-PROGRAMMED SERIES 20 PAL EQUIVALENTS |
| NATIONAL SEMICONDUCTOR CORP | 20-PIN PALs | BIPOLAR | VERY HIGH SPEED, HALF-, QUARTER-POWER VERSIONS |
| | 24-PIN PALs | BIPOLAR | ULTRAFAST, FAST, AND STANDARD VERSIONS |
| | PALC16F8 | FUSED CMOS | PAL COMPATIBLE WITH PROGRAMMABLE OUTPUTS |
| | ECL PALs | BIPOLAR | 20- AND 24-PIN PLDs IN ECL TECHNOLOGY |
| | PL21F10 | BIPOLAR | ASYNCHRONOUS, REGISTERED FPLA WITH PROGRAMMABLE OUTPUT |
| PANATECH SEMICONDUCTOR | 20-PIN PALs | EPROM CMOS | PAL-COMPATIBLE WITH PROGRAMMABLE OUTPUT POLARITY |
| SIGNETICS CORP | PROGRAMMABLE GATE ARRAYS | BIPOLAR | ONE (AND) LOGIC ARRAY, 20- AND 28-PIN VERSIONS |
| | ADDRESS DECODERS | BIPOLAR | ONE (AND) LOGIC ARRAY, 24-PIN VERSIONS |
| | FPLAs | BIPOLAR | 20-, 24-, AND 28-PIN PLDs WITH FEEDBACK TERMS |
| | FPLSs | BIPOLAR, EPROM CMOS | FPLA WITH REGISTERS (BURIED AND OUTPUT), FEEDBACK |
| SPRAGUE SOLID STATE | 20-PIN PALs | EPROM CMOS | COMPATIBLE WITH 16LC8, 16RC8, 16RC6, AND 16RC4 PALs |
| TEXAS INSTRUMENTS INC | 20-PIN PALs | BIPOLAR | VERY HIGH SPEED (IMPACT) AND HALF-POWER VERSIONS |
| | 24-PIN PALs | BIPOLAR | VERY HIGH SPEED (IMPACT) AND REGISTERED VERSIONS |
| | FPLAs | BIPOLAR | 3-STATE (-839) OR OPEN-COLLECTOR (-840) OUTPUTS |
| | FPLSs | BIPOLAR | FPLA WITH REGISTERS (BURIED AND OUTPUT), FEEDBACK |
| VLSI TECHNOLOGY INC | EPL FAMILY | EPROM CMOS | COMPATIBLE WITH 20-PIN PALs |
| | VP16RP8M | MASKED CMOS | HARD-WIRED REPLACEMENT FOR 20- AND 24-PIN PALs |
| | VP16V8E, VP20V8E | EE CMOS | SUPERSET OF 20- AND 24-PIN PALs |
| XILINX INC | XC-2064 LCA | RAM-BASED CMOS | PROGRAMMABLE LOGIC CELLS AND INTERCONNECTS |

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| 50 | 1/MHz | FROM $6.44 (COMMERCIAL), $17.94 (HI-REL) | BOX 1239, MELBOURNE, FL 32901 | (305) 724-3576 | **CIRCLE NO 682** |
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| 50 MHz | 180 | $26.71 (1000) | | | |
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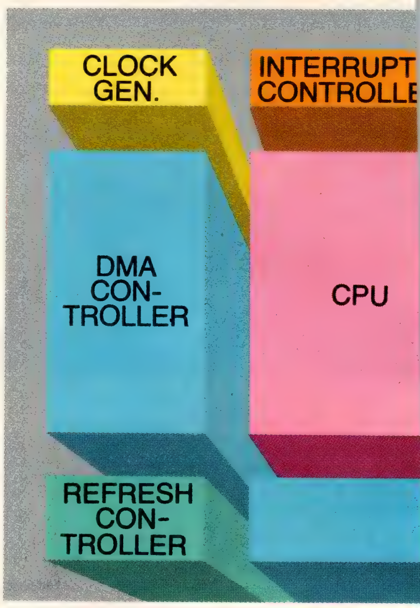
| 25, 35 | 90 | FROM $2 (5000) | | | |
| 20, 30 MHz | 20 | $55 | 2069 E HAMILTON AVE, SAN JOSE, CA 95125 | (408) 559-7778 | **CIRCLE NO 692** |

# Leading

# The new

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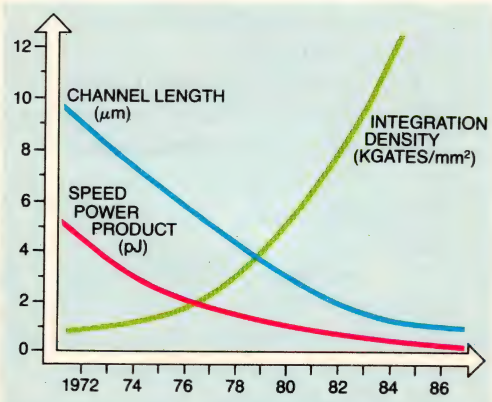


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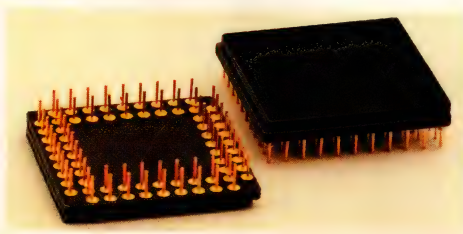

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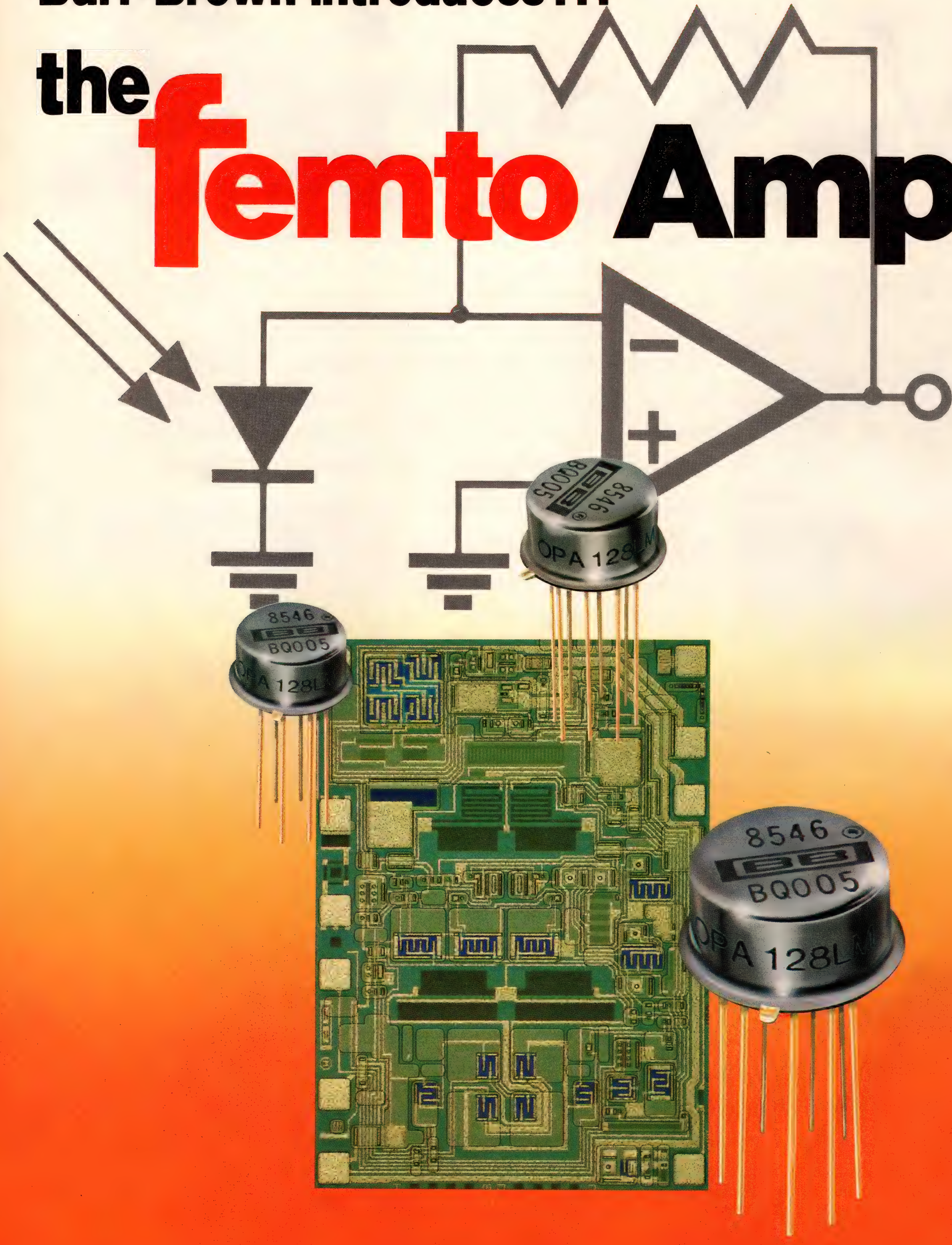

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Personal Computer Circuit Design Tools

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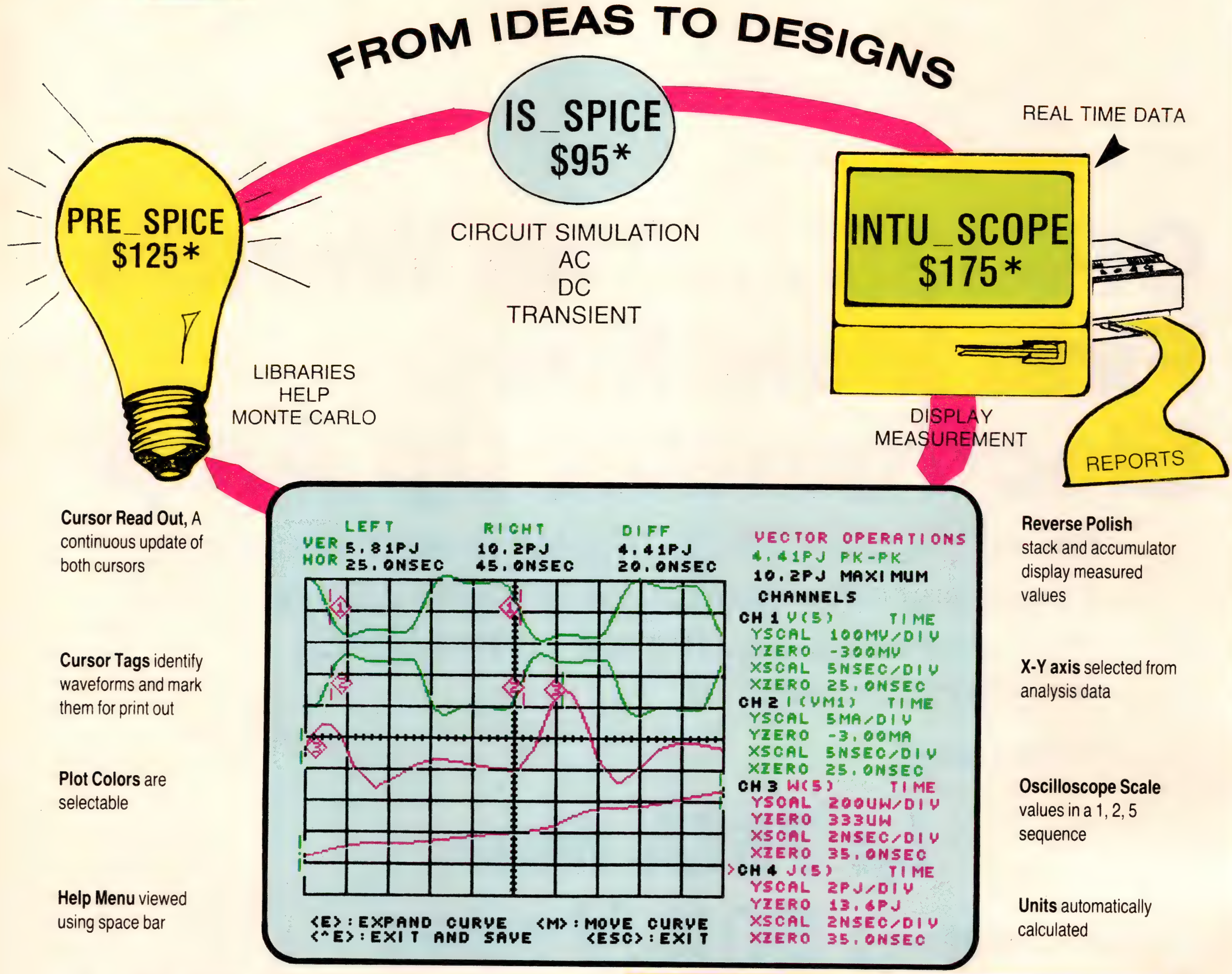


**Cursor Read Out,** A continuous update of both cursors

**Cursor Tags** identify waveforms and mark them for print out

**Plot Colors** are selectable

**Help Menu** viewed using space bar

**Reverse Polish** stack and accumulator display measured values

**X-Y axis** selected from analysis data

**Oscilloscope Scale** values in a 1, 2, 5 sequence

**Units** automatically calculated

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# Overcome electrical, thermal problems in high-power op amps

*A 1-chip power op amp is capable of driving ±35V at ±10A. This article, part 1 of a 2-part series, describes the electrical and thermal problems accompanying the use of such high-power devices and gives advice on how to solve the problems. Part 2 will present a variety of applications for the op amp.*

Robert Widlar and Mineo Yamatake,
*National Semiconductor Corp*

By understanding the practical problems associated with the use of a high-power operational amplifier, you can avoid such circuit problems as oscillation and distortion. Further, a study of the amplifier's thermal-protection characteristics allows you to make actual measurements of heat-sink design margins. The 150W LM12 is capable of supplying ±35V at ±10A; its peak-power rating of 800W makes the device capable of driving reactive loads. To obtain optimum performance from the amplifier, you should observe proper procedures for grounding, bypassing, loading, and providing efficient heat-sinking to the device.

Power op amps are subject to many of the same problems that general-purpose op amps experience. Excessive input or feedback resistance can cause a dc offset voltage on the output because of bias-current drops, or it can combine with stray capacitance to cause oscillations. Improper supply bypassing and capacitive loading, alone or in combination, can also result in oscillations. In many cases, you can avoid spending hours tracking down seemingly incomprehensible design problems by monitoring the op amp's output with a wideband oscilloscope.

For instance, when the LM12 op amp drives low-impedance loads and provides current transients greater than 10A, the effects of inductance and resistance of wire interconnects can become troublesome. Furthermore, in order to make the IC dissipate 90W continuously, you must mount it to an adequate heat sink.

The management and protection circuitry of the LM12 can also affect the system's operation. For example, if the total supply voltage exceeds ratings or drops below 15V, the op amp will shut off completely. Case temperatures above 150°C also cause complete shutdown until the temperature drops to 145°C. Reactivation of the op amp could take several seconds, depending on the heat-sink design. When the LM12's dynamic safe-area protection is activated, the main feedback loop loses control and output drive current is reduced. Oscillations may also result. In ac applications, the dynamic protection will cause waveform distortion.

To avoid spurious oscillation, you should bypass the op amp's supply terminals with low-inductance capaci-

*Power-amplifier circuitry demands that you use special care in grounding and bypassing and that you protect the amplifier from the effects of reactive loads.*

tors that have short leads and are located close to the package terminals. High-power op amps require larger bypass capacitors than do low-power units. The LM12 will be stable as long as you use good-quality electrolytic bypass capacitors whose values are greater than 20 μF. The current in the supply leads is a rectified component of the load current. Unless you provide adequate bypassing, this distorted signal can feed back into the op amp's internal circuitry. To obtain low distortion at high frequencies, you must bypass the supplies with capacitors of 470 μF or more at the package terminals.

With ordinary op amps, lead-inductance problems usually occur in inadequately bypassed supply leads. Power op amps are also sensitive to inductance in the output lead, particularly in the presence of heavy capacitive loading. To minimize common inductance with the load, you should connect feedback to the input directly from the output terminal. Make sure that when you use remote sensing, you provide a high-frequency feedback path directly from the output terminal.

Lead inductance can also cause voltage surges on the supplies. If the op amp has long leads to its power source, energy stored in the lead inductance when the output is short-circuited can get dumped back into the supply bypass capacitors upon removal of the short circuit. You can reduce the magnitude of this transient by increasing the size of the bypass capacitor near the IC. With 20-μF local bypass capacitors, these voltage surges are important only if the lead length exceeds a couple of feet (ie, when lead inductance is greater than 1 μH). Twisting together the supply and ground leads minimizes the transient effect.

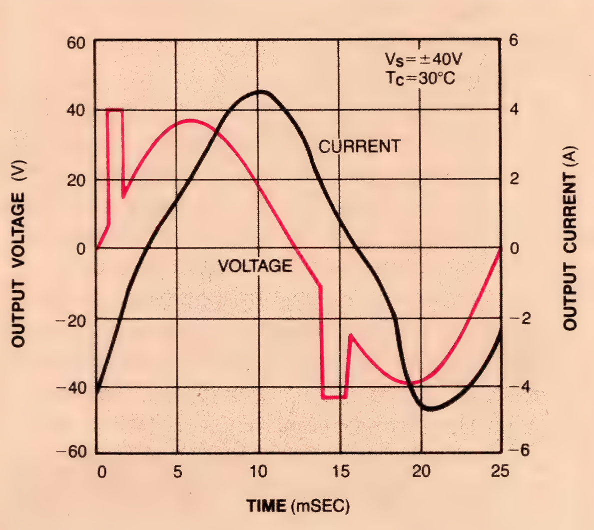


***Fig 1—Output voltage can exceed supply levels** when an op amp drives an inductive load. These curves show the activation of the LM12's dynamic safe-area protection. The stored energy in the inductor drives the output voltage beyond the supply levels.*

**Avoid ground loops**

In fast, high-current circuitry, various problems can arise from improper grounding. In general, you can avoid difficulties by returning all grounds separately to a common point. When such a connection is impractical, be sure to minimize the ground-path impedance for the supply bypasses, the load, and the input signal. To provide optimum grounding, use ground planes whenever possible.

Many problems unrelated to system performance are traceable to the grounding of line-operated test equipment that's used for system checkout. When you're using several pieces of test equipment, hidden paths are particularly difficult to sort out, but you can minimize the problem by using current probes or isolated oscilloscope preamplifiers. Eliminating any direct ground connection between the signal generator and the oscilloscope's synchronization input solves ground-feedback problems.

When a push-pull amplifier goes into power limit while driving an inductive load, the energy stored in the inductance can drive the output to voltages beyond the supply levels. **Fig 1,** for example, shows the overload response of an LM12 that's driving ±36V at 40 Hz into a 4Ω load in series with 24 mH.

The IC has internal supply-clamp diodes, but these clamps have a parasitic current that dissipates roughly half the clamp current across the total supply voltage. The internal protection circuitry can't control this dissipation; if the dissipation is sustained, the IC will experience catastrophic failure. You should, therefore, use external diodes to clamp the output to the power supplies.

Further, if you don't use external clamp diodes, a short circuit between the output and the supplies can induce random failures. Therefore, it's prudent to use output clamp diodes even when the load isn't obviously inductive. Failure of the IC is particularly violent when it's operating from low-impedance supplies: The $V^+$ pin can vaporize and blow a hole through the top of the can. If the LM12 fails, install diodes before you try again.

Because the clamp diodes clamp only current tran-

sients, they usually don't need heat sinking. When transients reach 15A, however, forward drop can reduce the efficacy of the clamp diodes. If the forward drop exceeds 0.8V, the clamp to the negative supply can lose some of its effectiveness. To reduce the diode's forward drop, mount this diode to the op amp's heat sink. A third diode ($D_3$ in **Fig 2**) will protect the amplifier in the unlikely case that $D_2$'s forward drop becomes excessive. For $D_3$ you must use a diode that's capable of dissipating a continuous power level that's

## A look at the LM12

The performance of the LM12 puts the op amp in a class with discrete and hybrid power amplifiers. The IC incorporates internal management circuitry that provides smooth turn-on and automatic protection against a variety of fault conditions; it offers instantaneous limiting of the power transistors' peak junction temperatures.

**Table 1** summarizes the LM12's performance. The op amp's input common-mode range extends to within 1V of the positive supply and to 3V above the negative supply. If the applied signal exceeds the input-voltage range, no input-polarity reversal occurs. If the signal drives the inputs beyond the supply voltages, no damage results.

The IC offers compensation for unity-gain feedback, and small-signal bandwidth is 700 kHz. The part's slew rate is 9V/µsec, even when the LM12 is connected as a follower. This slew rate translates to a 60-kHz power bandwidth under load with a ±35V output swing. The op amp is stable with or without capacitive loading; the maximum load capacitance depends upon loop gain. The IC exhibits no spurious output stage oscillations and requires no series-RC snubber on the output.

The LM12 delivers ±10A output current at any output voltage, yet is completely protected against output overloads, including short circuits to the supplies. Peak-temperature limiting within the power-transistor array provides dynamic safe-area protection. On-chip circuitry controls the IC's turn-on characteristics by keeping the output open-circuited until the total supply voltage reaches 15V. The output also becomes open-circuited when the case temperature exceeds 150°C or as the supply voltage approaches the $BV_{CEO}$ of the output transistors. The op amp withstands overvoltages as high as 100V.

The LM12's guaranteed power ratings are not established by statistical methods from sample tests. Instead, the manufacturer interpolates the ratings from actual measurements of power capability into thermal limit; these measurements are standard production tests for the op amp.

The LM12 is supplied in a steel TO-3 package with four through leads; the case is the $V^-$ connection. A gold-eutectic die-attach and a molybdenum interface let the op amp avoid thermal-fatigue problems under power-cycling conditions. Two voltage grades (60 or 80V total supply span) are available; both are specified for either the military or industrial temperature range.

### TABLE 1— TYPICAL CHARACTERISTICS OF THE LM12

| PARAMETER | CONDITIONS | VALUE |
|---|---|---|
| INPUT OFFSET VOLTAGE | $V_{CM} = 0$ | 2 mV |
| INPUT BIAS CURRENT | $V_{CM} = 0$ | 150 nA |
| VOLTAGE GAIN | $R_L = 4\Omega$ | 50V/mV |
| OUTPUT-VOLTAGE SWING | $I_{OUT} = \pm 1.5A$<br>$\pm 10A$ | ±38V<br>±35V |
| PEAK OUTPUT CURRENT | $V_{OUT} = 0$ | ±13A |
| CONTINUOUS DC DISSIPATION | $T_C =$ 25°C<br>100°C | 90W<br>55W |
| PULSE DISSIPATION | $T_{ON} =$ 10 mSEC<br>1 mSEC<br>0.2 mSEC | 120W<br>240W<br>600W |
| POWER OUTPUT | $R_L = 4\Omega$ | 150W |
| TOTAL HARMONIC DISTORTION | $R_L = 4\Omega$ | 0.01% |
| BANDWIDTH | $A_V = 1$ | 700 kHz |
| SLEW RATE | $R_L = 4\Omega$ | 9V/µSEC |
| SUPPLY CURRENT | $I_{OUT} = 0$ | 60 mA |

*The thermal and protection circuitry in a power op amp is crucial to the part's survival in situations that produce excessive junction-temperature rise.*

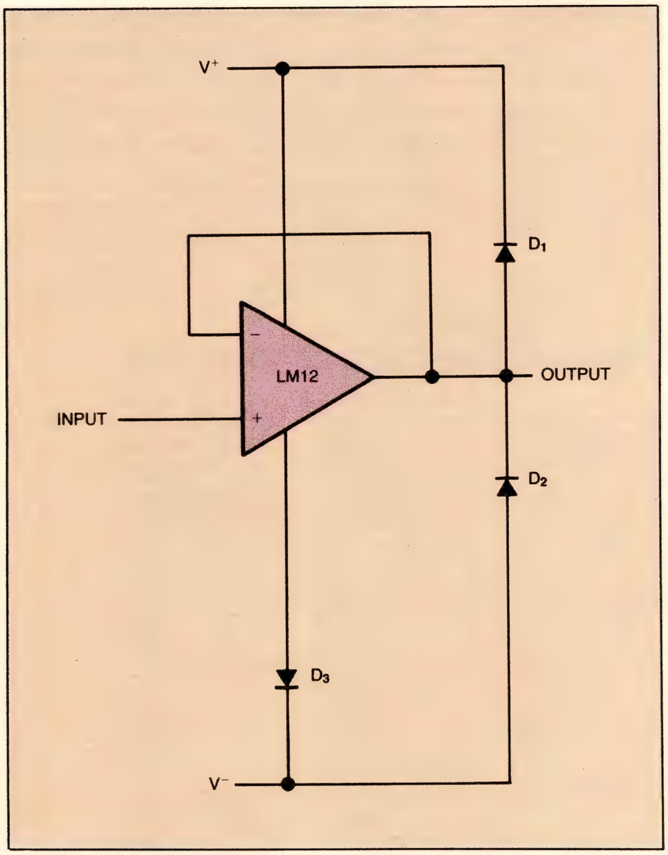


***Fig 2—Output clamp diodes $D_1$ and $D_2$ dump inductive-load current*** *into the supplies when the op amp goes into power-limit mode. You might need to use the third diode, $D_3$, if $D_2$'s forward drop is excessive.*

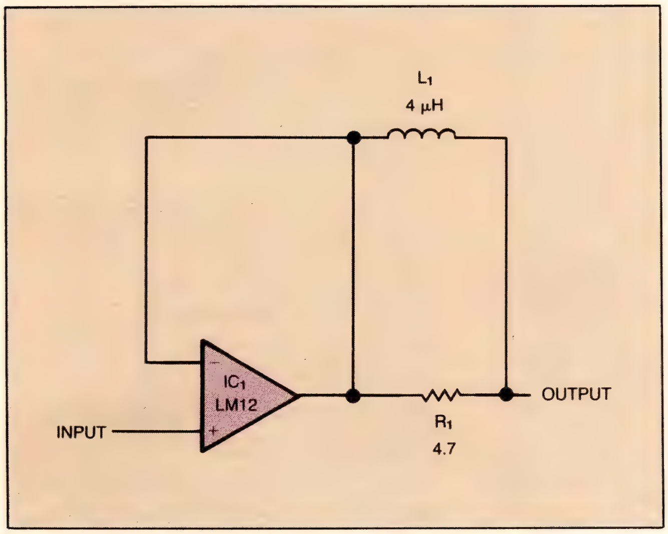


***Fig 3—Use an inductor to isolate capacitive loads.*** *The noninductive resistor prevents resonance problems by killing the Q of the series-resonant circuit.*

determined by the negative supply current of the op amp.

The LM12 is normally stable when it drives resistive, inductive, or small capacitive loads. Large capacitive loads would interact with the open-loop output resistance (about 1Ω), reducing the phase margin of the feedback loop and ultimately causing oscillation. The critical capacitance depends upon the feedback applied around the amplifier: A unity-gain follower can handle about 0.01 μF, while more than 1 μF doesn't cause problems as long as the loop gain doesn't go below 10. If you configure the op amp for loop gains greater than unity, you can enhance the stability of the closed-loop circuit by placing a speed-up capacitor across the feedback resistor.

In all cases, the op amp will behave predictably only if the supplies are properly bypassed, ground loops are controlled, and high-frequency feedback derives directly from the output terminal. Further, so-called capacitive loads are not always purely capacitive. A high-Q capacitor in combination with long leads can present a series-resonant load to the op amp. In practice, this LC load is not usually a problem, but you should keep the possibility in mind.

You can accommodate large capacitive loads (including series-resonant LC loads) by isolating the feedback amplifier from the load as shown in **Fig 3.** The inductor gives low output impedance at low frequencies while providing an isolating impedance at high frequencies. The resistor kills the Q of series-resonant circuits that are formed by capacitive loads. This resistor should be a low-inductance, carbon-composition resistor. The optimum values for the inductor and resistor depend upon the feedback gain and expected nature of the load, but tolerance need not be tight. You can make a 4-μH inductor by winding 14 closely spaced turns of number 18 wire around a 1-in.-diameter form.

You can stabilize the LM12 for all loads by using a large capacitor on the output, as **Fig 4** shows. This compensation gives the lowest possible closed-loop output impedance at high frequencies and the best load-transient response. The method is suitable for use in voltage regulators.

A feedback capacitor, $C_1$, connects directly to the output pin of the IC. The output capacitor, $C_2$, is connected at the output terminal with relatively short leads. Use single-point grounding to avoid dc and ac ground loops.

The impedance $Z_1$ is that of the wire connecting the op amp's output to the load capacitor. About three

inches of #18 wire (70 nH) provides stability; an 18-in. length (400 nH) begins to degrade load-transient response. If you use a plastic-film or solid-tantalum capacitor with an equivalent series resistance (ESR) of 0.1Ω, the minimum load capacitance is 47 μF. Aluminum electrolytic capacitors work as well, although you have to increase their capacitance to about 200 μF to bring ESR below 0.1Ω.

Loop stability is not the only gremlin in op amps that drive reactive loads. Time-varying signals can cause the part's power dissipation to increase markedly, particularly when the op amp experiences the combination of capacitive loads and high-frequency excitation.

### Input compensation provides stability

If the LM12's high-frequency loop gain is near unity, the op amp is prone to low-amplitude oscillation bursts when it comes out of saturation. The voltage-follower connection is more susceptible than other connections to such oscillation. You can eliminate this glitching—at the expense of small-signal bandwidth—by using input compensation. You can also use input compensation in combination with LR load isolation to improve capacitive-load stability.

**Fig 5a** shows an example of a voltage follower that uses input compensation. The $R_2$-$C_2$ combination across the input works with $R_1$ to reduce feedback at high frequencies without greatly affecting response below 100 kHz. A lead capacitor, $C_1$, improves phase margin at the unity-gain crossover frequency. Optimum operation of the circuit requires that the output impedance of the circuitry driving the follower be well below 1 kΩ even at frequencies as high as a few hundred kilohertz.

**Fig 5b** shows the application of input compensation in an integrator configuration. Both the follower and the integrator can handle 1-μF capacitive loading without LR output isolation.

To make optimum use of the LM12, you should understand the nature of the op amp's temperature-limiting mechanism. The LM12's output transistors can dissipate power until their peak junction temperature reaches 230°C (±15°C). When this temperature is reached, internal limiting circuitry takes over, regulating peak temperature. **Fig 6,** which gives the peak output-current waveform with the output instantaneously short-circuited to ground, shows how the limiting works. Conventional current limiting holds the short-circuit current near 13A for a few hundred microseconds, then temperature limiting takes over as junction temperature tries to rise above 230°C. The response

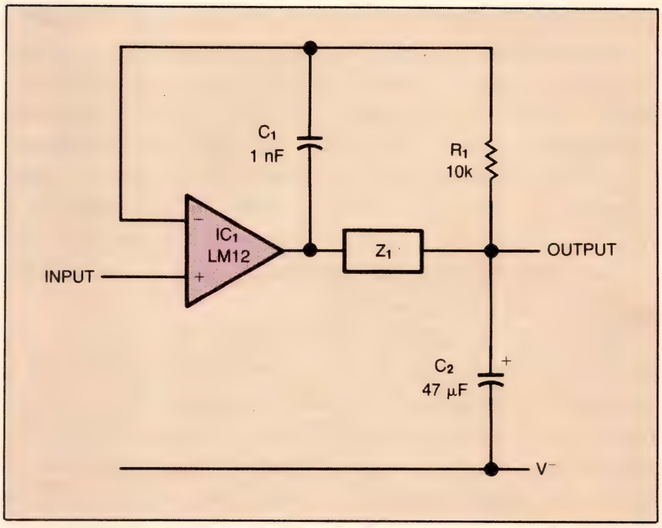


***Fig 4—A large output capacitor stabilizes the op amp*** *for all loads. The impedance $Z_1$ is that of the wire that connects the IC's output to the load-capacitor terminal.*

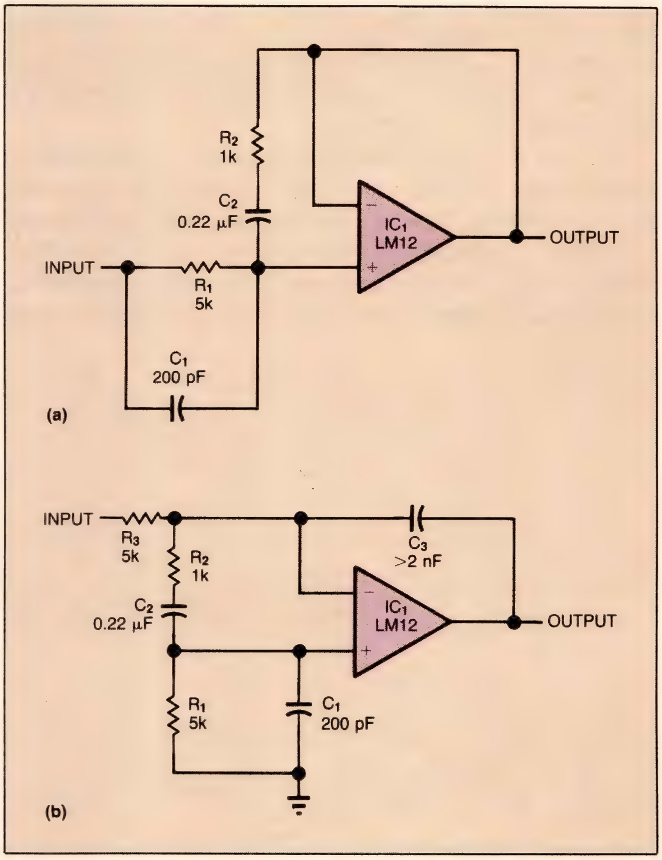


***Fig 5—Input compensation reduces bandwidth and increases stability*** *in low-gain configurations. The method helps stabilize the op amp against capacitive loads for the follower in **a** and for the inverter in **b**.*

*Lead inductance and capacitive loading form an insidious alliance that, uncorrected, can cause problems ranging from instability to destruction of the op amp.*

time of the temperature limiter is well below 100 μsec.

Because the IC uses this peak-temperature limiting scheme, its power capabilities depend on case temperature, transistor operating voltages, and the way the dissipation varies with time. For two case temperatures, **Fig 7** shows the amplitude of the power pulse required to activate power limiting in 100 msec as a function of collector-emitter voltage on the output transistors. The continuous dissipation limit is about 15% less than the 100-msec limit.

The pulse capabilities of the output transistors are shown in **Fig 8.** The curves give the amplitude of a constant-power pulse required to activate power limiting in the indicated time. When the pulse widths are longer than 1 msec and the collector voltages are above 40V, the pulse capability decreases, as the figure shows.

The guaranteed power ratings of the LM12 are based on a peak junction temperature of 200°C instead of the 230°C limiting temperature. The IC's specs also take test accuracy, guard bands, and unit-to-unit variations into account. The result is that the guaranteed ratings are about 40% lower than those required to activate the thermal-limit mechanism.

The worst-case, safe-area curves for a peak junction temperature of 200°C and a 25°C case temperature are shown in **Fig 9a.** The guaranteed-maximum dc thermal resistance is given as a function of collector-emitter voltage in **Fig 9b.** You can see from these curves that the increase in thermal resistance with voltage is much smaller at higher case temperatures. Finally, **Fig 9c** shows the equivalent thermal resistance for power pulses. Again, these are worst-case numbers. The voltage dependency of thermal resistance in **Fig 9c** is for a 25°C case temperature. At higher case temperatures, this dependency is more moderate **(Fig 9b).**

Under the condition of ac loading, both power transistors share the dissipation, and the worst-case thermal resistance can drop to 1.9°C/W. However, the frequency of the signal must be high enough that the junction temperature doesn't exceed the peak ratings of either output transistor.

**Derate the maximum junction temperature**

It's not unusual for designers to derate the maximum junction temperature of semiconductors below the manufacturer's specified value. In general, the junction-temperature limit for power semiconductors is 200°C, although standard junction-temperature limits for hermetic or plastic packages might differ.

The LM12 can operate continuously at 200°C. Such conditions as out-of-spec line voltage or lack of air circulation would cause the equipment to stop working temporarily; the part would not suffer excessive stress or catastrophic failure. In certain applications, however, a temporary shutdown can have the same effect as a permanent one; you should definitely use derating in such applications.

Modern IC power transistors don't experience catastrophic failure over a short term, even when peak

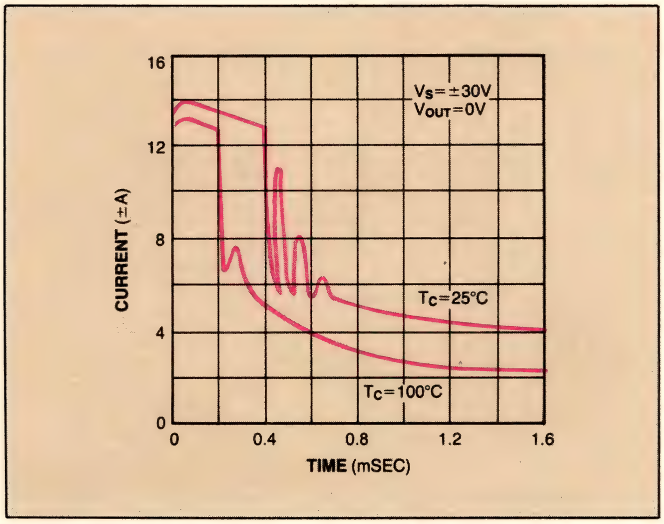


***Fig 6—Internal limiting circuitry regulates peak temperatures** in the LM12. The circuit reduces output short-circuit current when the transistors' junction temperature reaches 230°C.*

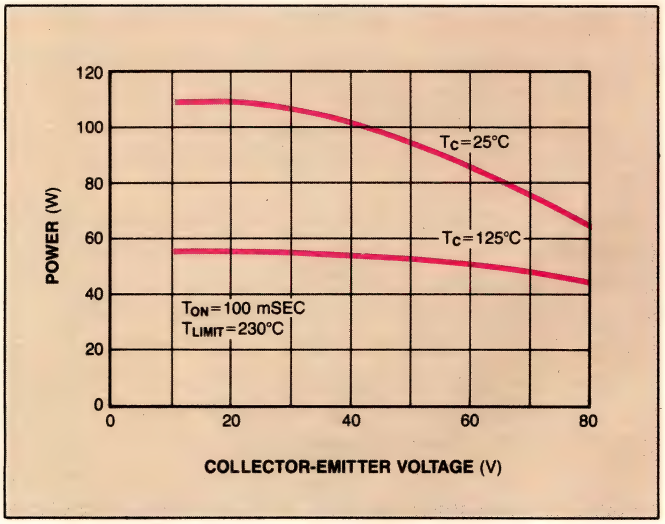


***Fig 7—The power required to activate the power-limit mode** in the LM12 is lower for higher collector-emitter voltages, but the drop-off diminishes for very high case temperatures.*

## A power IC's thermal aspects

In a power IC, the peak junction temperature occurs at the center of the power transistor. At the edge of the power transistor, the temperature rise (junction-to-case) is only 60% of that at the center. **Fig A** shows the surface-temperature profile, moving out from the center of the power transistor, for a situation in which the peak junction temperature is 200°C and the case temperature is 75°C. In this idealized 2-dimensional plot, the temperature at the edge of the power array is only 160°C.

In real situations, the temperature falloff can be considerably greater than that indicated by the curve. Earlier IC designs have located the sensor several mils away from the power array. As a result, the temperature sensor responds to about 30% of the temperature rise in conventional power-IC designs.

Truly effective temperature sensing requires a sensor that is distributed throughout the power array, yet responds to the peak temperature almost instantaneously. In the LM12 design, these requirements are met by a thermal-sense emitter, located a fraction of a mil from the active emitter, that winds through the entire power array.

In ICs using conventional thermal limiting, the output transistors' junction temperature is controlled at lower case temperatures via foldback current limiting, which restricts power dissipation. When case temperature rises to a certain level, the thermal-limiting mechanism is activated. In general, the peak limiting temperature will be substantially greater than the thermal limit, because the sensor doesn't respond to the full temperature rise.

**Fig B** is an idealized plot of peak junction temperature for increasing case temperature. The plot is drawn with the assumption that the thermal limit is 150°C, rise in power-limit mode is 150°C, and the thermal sensor responds to one-third the peak temperature. These operating conditions are typical for many IC designs.

Because of the tolerances involved in a practical foldback-current-limit design, worst-case dissipation in such a design can be twice the typical values. Further, such designs are subject to non-ideal 3-dimensional effects. Peak junction temperatures well above 300°C can occur in ICs that use conventional limiting techniques. Peak-temperature sensing, however, makes foldback current limiting unnecessary: The power transistor can handle full rated voltage and current simultaneously, yet be fully protected.

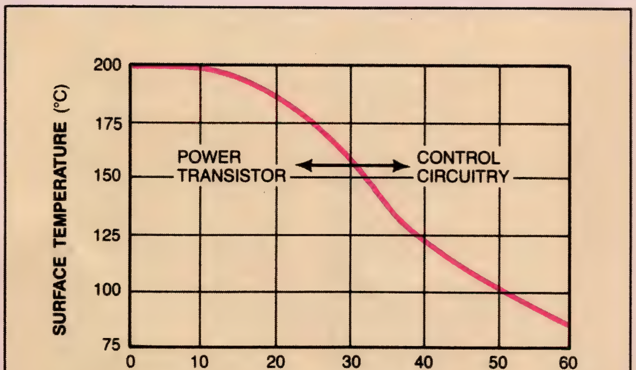


***Fig A—In a power IC, peak temperature occurs at the center** of the power transistor. The IC's surface temperature drops, going from the center of the power transistor out into the control circuitry. The active emitters at the edge of the power array are at x=0.*

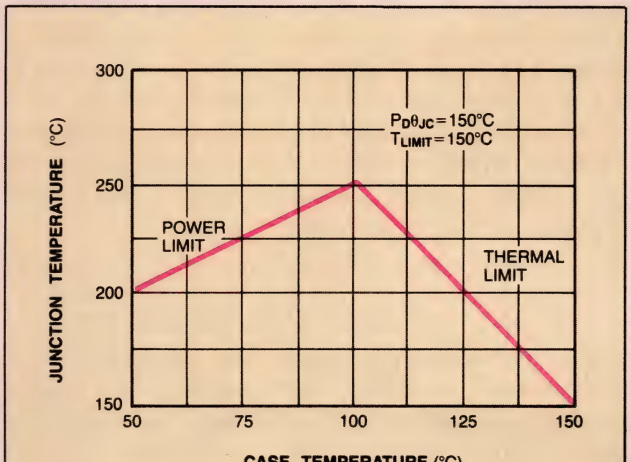


***Fig B—In many ICs, maximum thermal stress doesn't occur** in the absence of a heat sink, as this plot indicates.*

*To determine the heat sinking needed for a power op amp, you must understand the temperature profiles on the surface of the op amp's die.*

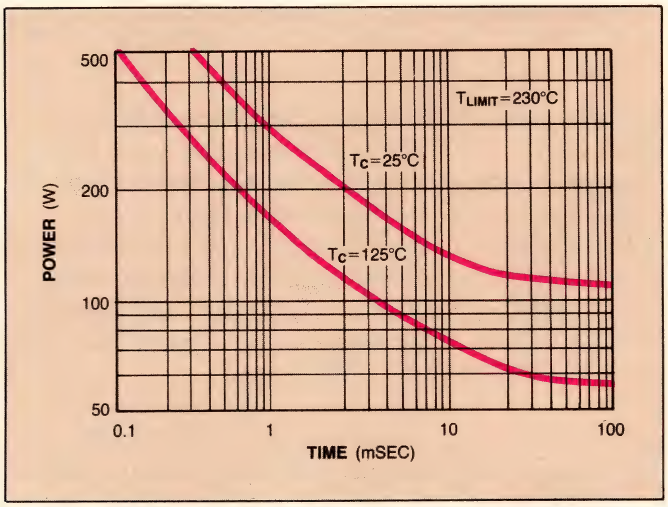


***Fig 8—The peak-dissipation capability** of the LM12 depends on pulse duration. For pulses wider than 100 msec, the external heat sink determines the ratings.*

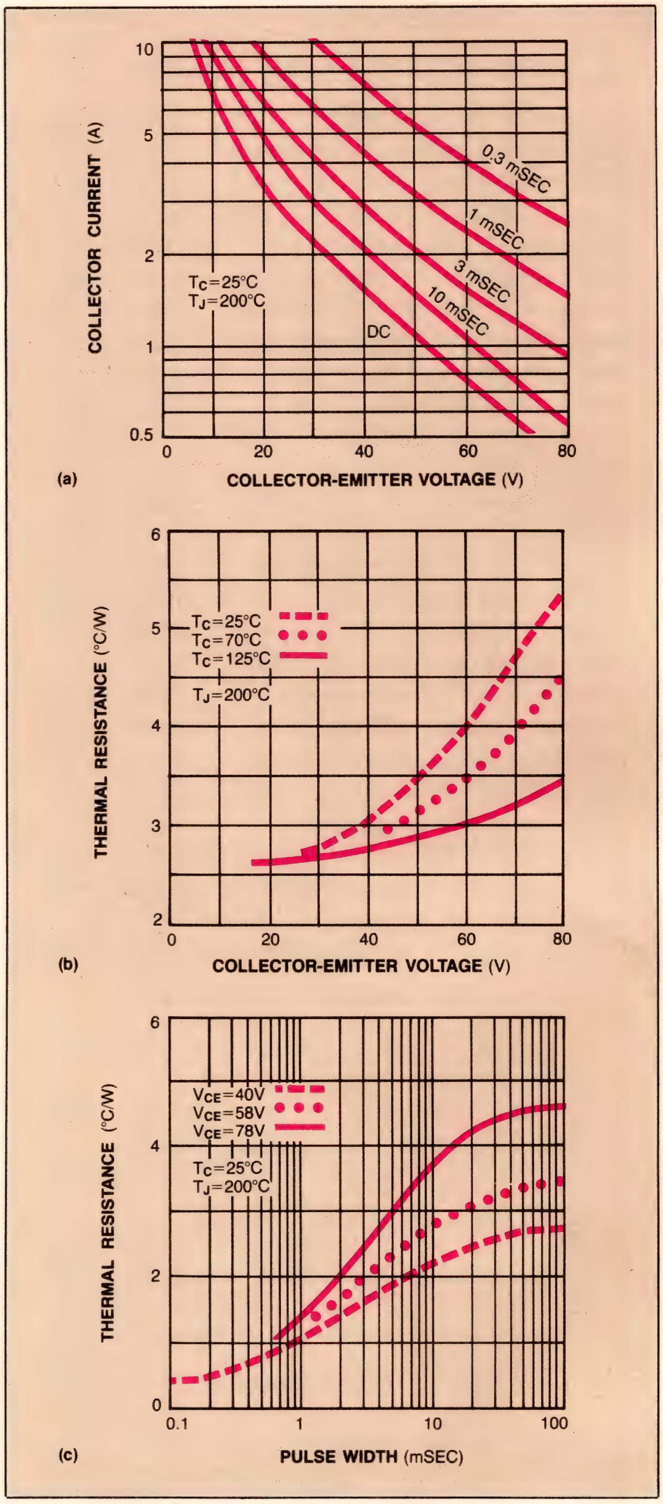


***Fig 9—Three thermal curves characterize the LM12's power ratings.** The curves are the safe-area plot **(a)**, the change in dc thermal resistance with temperature and operating voltage **(b)**, and the pulse thermal resistance **(c)**.*

junction temperatures reach 300°C. However, power cycling can cause problems. For example, in power transistors having a soft-solder die-attach, die-attach failures can take place after 30,000 cycles and a 70°C temperature rise. The LM12 avoids such failures by using a gold-eutectic die-attach and a molybdenum spacer. Even so, when dissipating 200W, the LM12 has exhibited metallization failures after one million cycles from 50°C to power limit at 230°C.

Thermal derating is more important for the op amp's control circuitry than for its power transistors. Operating the control circuitry at temperatures above 150°C can affect reliability. Fortunately, the control circuitry is exposed to only a fraction of the temperature rise in the power transistors. You can base derating on a thermal resistance of 0.9°C/W, independent of operating voltage. With ac loading, where power dissipation occurs in both power transistors, this thermal resistance drops, finally approaching 0.6°C/W.

The LM12's ratings are based on the case temperature as measured on the bottom of the TO-3 package near the center. To minimize the thermal resistance between this region and the heat sink, you must be sure to mount the IC correctly. For example, when mounting the package directly to the heat sink, you should use a good thermal compound such as Wakefield Type 120 or Thermalloy Thermacote. Without this compound, thermal resistance will be no lower then 0.5°C/W, and it may be much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming that the package and the heat sink have <0.005-in. combined

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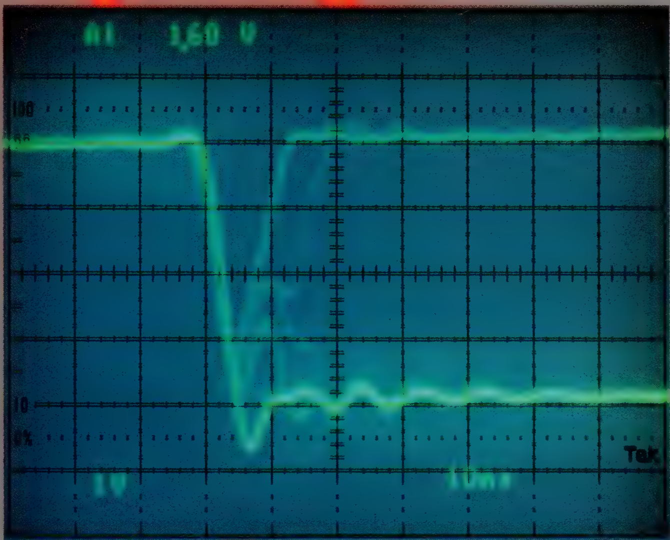

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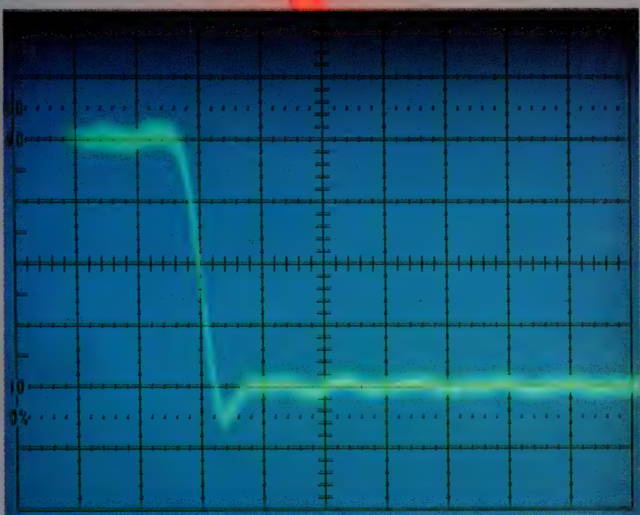

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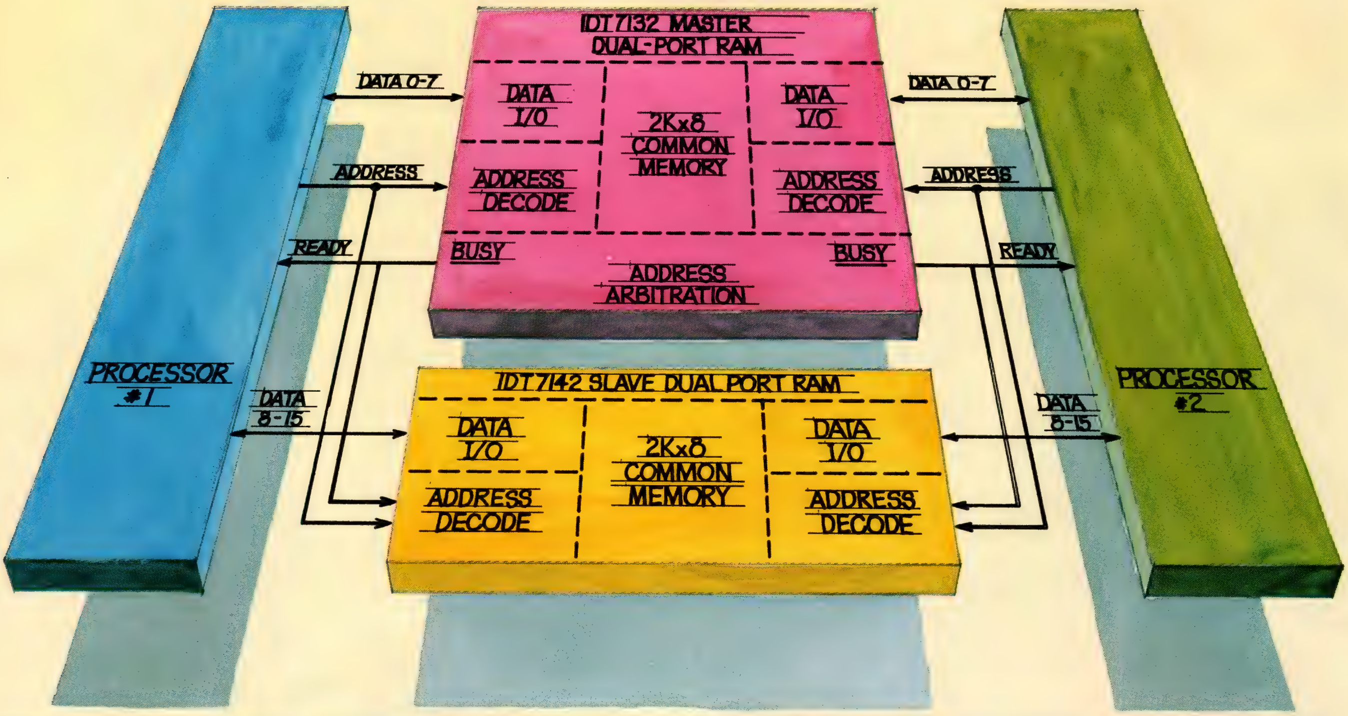


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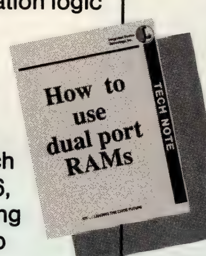


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| **16Ks** | | |
| 16Kx1 | IDT6167A | 25ns |
| 4Kx4 | IDT6168A | 25ns |
| 4Kx4 | IDT71681A* | 25ns |
| 4Kx4 | IDT71682A** | 25ns |
| 2Kx8 | IDT6116A | 35ns |
| **64Ks** | | |
| 64Kx1 | IDT7187 | 35ns |
| 16Kx4 | IDT7188 | 35ns |
| 16Kx4 | IDT7198*** | 35ns |
| 16Kx4 | IDT71981* | 35ns |
| 16Kx4 | IDT71982** | 35ns |
| **Dual Port Static RAMs** | | |
| 1Kx8 | IDT7130 MASTER | 55ns |
| 2Kx8 | IDT7132 MASTER | 55ns |
| 1Kx8 | IDT7140 SLAVE | 55ns |
| 2Kx8 | IDT7142 SLAVE | 55ns |

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*When you use a heat sink with a high-power amplifier, you must take care to minimize the thermal resistance between the amplifier's case and the heat sink.*

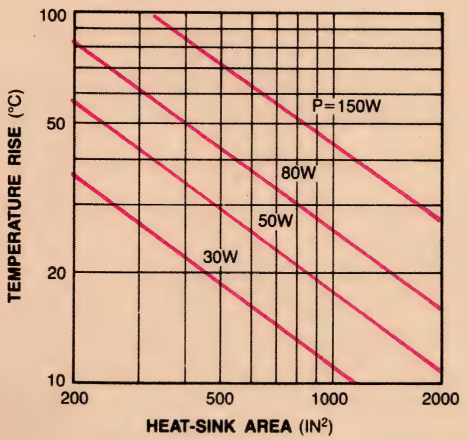


***Fig 10—You need a heat sink** to cool the LM12's package. These curves give the rise in case temperature as a function of heat-sink fin area; the curves assume that the part uses convection cooling.*

flatness run-out. Proper torquing of the mounting bolts is also important: You should use four to six inch-pounds of torque.

If you must isolate $V^-$ from the heat sink, you must use an insulating washer. If you use hard washers made of beryllium oxide, anodized aluminum, or mica, you must use thermal compound on both faces. Two-mil mica washers are the most common; they yield about 0.4°C/W interface resistance when you use them with the compound. Silicone-rubber washers are also available. Some vendors claim their rubber washers offer 0.5°C/W thermal resistance without thermal compound. Note, however, that these rubber washers deteriorate; you must replace them if you remove the IC.

### Choose the right heat sink

You'll need to attach a heat sink to the LM12, because without one, the op amp (with ±40V supplies and no load) can experience an internal temperature rise as high as 160°C. The types most suitable for dissipation of about 50W are made from an extruded aluminum channel equipped with multiple fins. It's important for you to choose a heat sink that has enough metal under the package to conduct heat from the center of the package bottom to the fins without introducing excessive temperature drop.

The power rating of a multifinned heat sink is determined largely by the surface area that's subject to convection cooling and by the allowable temperature rise to ambient. Heat loss from radiation can also be an important factor in simple heat sinks. However, for a heat sink in which multiple fins radiate toward each other, the radiation term is insignificant. Nevertheless, heat sinks are usually black anodized to maximize radiated heat.

**Fig 10** lets you estimate fairly accurately the surface area required for a given temperature rise and power dissipation. The heat sink's orientation, length, and fin spacing affect the area efficiency. The curves are drawn with the assumption that the surfaces are located in a vertical plane. If the surfaces are horizontal, the temperature rise increases by, say, 20%. Vertical dimensions longer than 4 in. are less efficient. Commercial heat sinks are normally designed so that fin spacing is not close enough to affect the performance shown in **Fig 10.**

It's not possible to specify an unqualified thermal resistance for a convection- or radiation-cooled heat sink. Both mechanisms will give a lower thermal resistance when temperature rise increases, and heat losses from radiation also increase as absolute temperature increases. Because radiation losses are not dominant in multifinned heat sinks, power dissipation and temperature rise characterize performance. You can drastically reduce heat-sink size by using forced-air cooling. **EDN**

## Authors' biographies


*Robert Widlar is a freelance linear-IC design consultant for National Semiconductor Corp (Santa Clara, CA). Designer of the legendary 702 and 709 monolithic op amps in a previous position at Fairchild Semiconductor (Mountain View, CA), Bob now lives in Puerto Vallarta, Mexico.*

*Mineo Yamatake has designed linear ICs at National Semiconductor (Santa Clara, CA) for the past 19 years. Before joining the company, he performed the same function at Fairchild Semiconductor (Mountain View, CA). Mineo's spare-time pursuits include fishing and mountain biking.*

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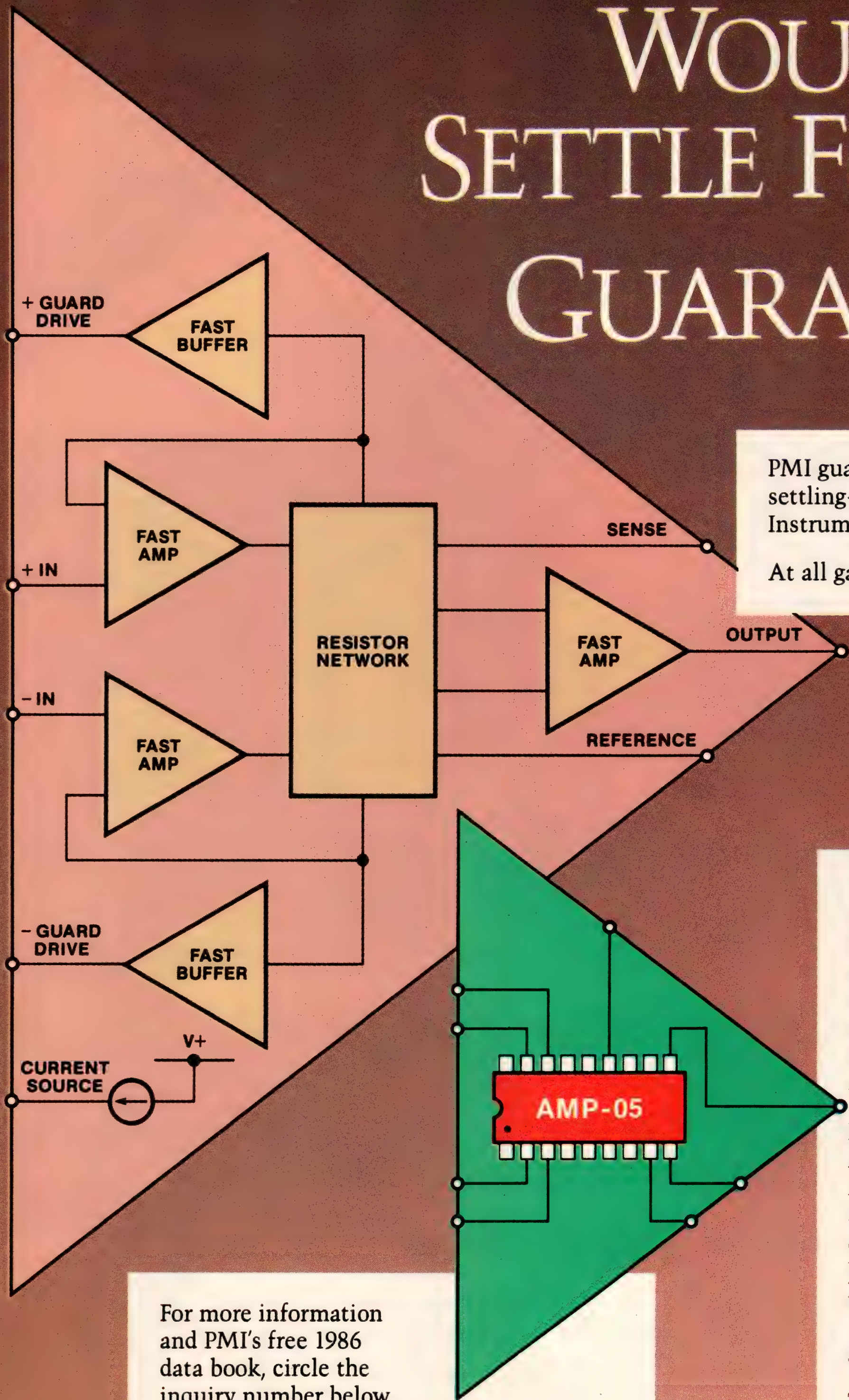


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# Use a PC to generate analog output signals

*An inexpensive system that controls analog output signals is easy to build with a personal computer, a D/A converter, and some interface circuitry. You can easily write the necessary control software for such computers as the Apple II and the IBM PC.*

John Croteau and Doug Grant,
*Analog Devices*

You can use a personal computer to control analog output signals. With a PC, a D/A converter, and some interface circuitry, for example, you can build an inexpensive system that can control wide-range frequency generators for waveforms or a system that tests analog ICs by applying precisely controlled dc signals to one or more input terminals of a device and monitoring the resulting output signals.

If you were to buy either a complete system, including a PC, or a plug-in board that's bus-specific to a PC that you already have, you'd probably pay for capabilities you don't need. However, if you develop a custom interface by putting D/A converters, op amps, and digital ICs on a board that you can plug into your PC, you'll obtain only the features that your application needs, and the cost will be relatively low.

One of the biggest considerations you'll have when designing your system will be to choose the right D/A converter for your application (see **box** "Understanding D/A converter specifications"). A D/A converter, like any other peripheral device, communicates with your PC either through an I/O port or through a memory location that the CPU can address directly but that doesn't contain any read/write memory. Usually, a D/A converter includes on-chip data latches so that it can recognize that it's being addressed and can accept data.

Depending on the converter you use, you may need some interface circuitry between the converter and the computer. This circuitry, which would consist of a few logic gates, would define the address for the D/A converter, and would match the timing requirements of the converter to those of the CPU and bus. The interface will be simplest when the CPU bus is wide enough to load all bits of the converter in parallel; in that case, you'll need only one memory or I/O address. However, when you're loading a 12-bit D/A converter from an 8-bit CPU (such as the 8080 or Z80 of a CP/M machine, the 6502 of an Apple II or IIe, or the 8088 of an IBM PC), your interface will need two separate sets of latches, each with its own address, and you'll have to program the CPU to load the data word in two portions.

For example, you might load the four least significant bits (LSB) through the upper nibble of the first I/O or memory address (with zeros in the lower nibble), and the eight most significant bits (MSB) through the second address, so that the data is left-justified. Some converters may require the reverse procedure; that is, they may require you to load the eight LSB through one

*The double-buffered input structure of modern D/A converters lets you interface them easily to computer buses of any width.*

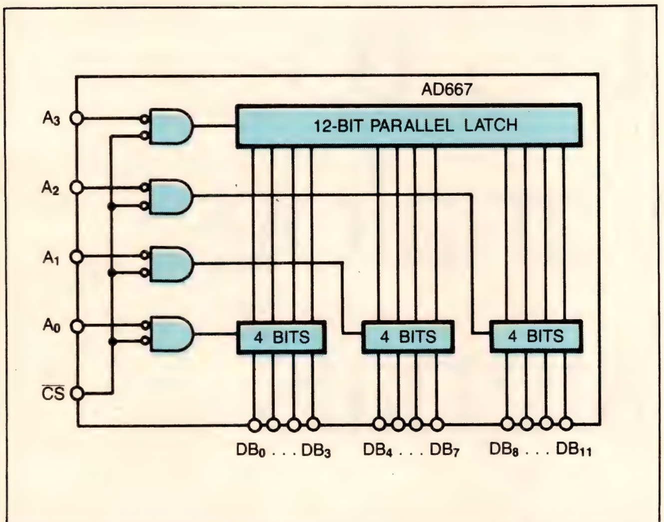


***Fig 1—Its double buffering allows you to preload the AD667 D/A converter** in sections from a μP bus of any width and then transfer the 12-bit input word to a second buffer for conversion.*

address and load four zeros (in the upper nibble) and the four MSB (in the lower nibble) through the other address. Data loaded in this manner is right-justified.

The double-buffered structure of modern D/A converters, such as the AD667 (**Fig 1**), provides a flexible, general-purpose interface to either 8- or 16-bit buses. A chip-select $\overline{CS}$ input, decoded from the high-order address bits, enables all of the input circuitry, which consists of a 12-bit second-rank register that holds the data to be converted, three 4-bit latches that you can load individually or in combination, and control logic that selectively enables the internal latches.

You load the 4-bit latches in one, two, or three operations, depending upon the width of the μP bus; then you strobe this data into the 12-bit buffer with a further I/O operation. An advantage of this structure is that you can arrange for several converters to share the address that controls the transfer of data from first-rank buffer to active buffer. You can preload each

## Understanding D/A converter specifications

A D/A converter is basically a digitally controlled current or voltage source whose analog output is a normalized fraction of its full-scale setting. Ideally, that fraction should be capable of taking on an infinite number of values, thus generating a continuous analog output function. However, the digital input offers only $2^N$ values for a word N bits in length. The analog output, therefore, is quantized with code-to-code steps equal to $2^{-N}$ of full scale, or 1 LSB. This resolution, which is a function of the number of bits in the input word, can be expressed in bits, decibels, percent, or parts per million.

Resolution in no way implies accuracy, however. In some applications, resolution is more important than accuracy; in others the reverse is true. The transfer curve of an ideal D/A converter is a set of points in which each point falls on a straight line from zero to full scale, and in which the difference between any two adjacent points is equal to 1 LSB. Four error terms describe a converter's accuracy, or deviation from the ideal: offset, gain error, integral nonlinearity (INL), and differential nonlinearity (DNL). Offset is the output's deviation from zero when the digital input calls for zero output; it affects all codes by the same additive amount. Gain error is the error in the slope of the transfer curve; it affects all codes by the same percentage amount. The user can compensate for both offset and gain error in hardware or software.

The user can't easily compensate for INL and DNL, however, so these characteristics determine the converter's performance limitations. INL specifies the transfer curve's deviation from an ideal straight line; DNL is the deviation of any measured code-to-code transition from the ideal value of 1 LSB. For example, if the difference in analog output values for two adjacent digital codes is only ⅓ LSB instead of 1 LSB, the DNL error is −⅔ LSB. If the D/A converter's output either increases or remains constant as the digital input increases, the converter is said to be monotonic. Monotonicity, therefore, implies a negative DNL of less than 1 LSB.

Some applications, such as digital audio applications, require better resolution than accuracy. The human ear can easily distinguish the difference in clarity between 10, 12, 14, and 16 bits of digitized sound, but it usually can't detect the distortion resulting from nonmonotoni-

converter in turn with the appropriate digital values, so that when you execute the transfer instruction, all analog outputs will assume the correct values at the same time.

The timing requirements of the AD667 are simple **(Fig 2)**. The logic that generates the control signals must decode enough address bits to ensure that the converter will not be accessed inadvertently and that the chip-select line will not be activated until the address lines have stabilized with a valid address. The $\overline{CS}$ signal must be held active for at least 100 nsec, but the data need only be valid during the last 50 nsec of that period. The trailing edge of the $\overline{CS}$ signal strobes the data from the bus into the addressed section or sections of the first-rank buffer.

Either an Apple II computer **(Fig 3)** or an IBM PC **(Fig 4)** can easily fulfill these timing requirements. All I/O ports in the Apple II are memory mapped, so you can use the $\overline{\text{DEV SEL}}$ line to represent a decoded

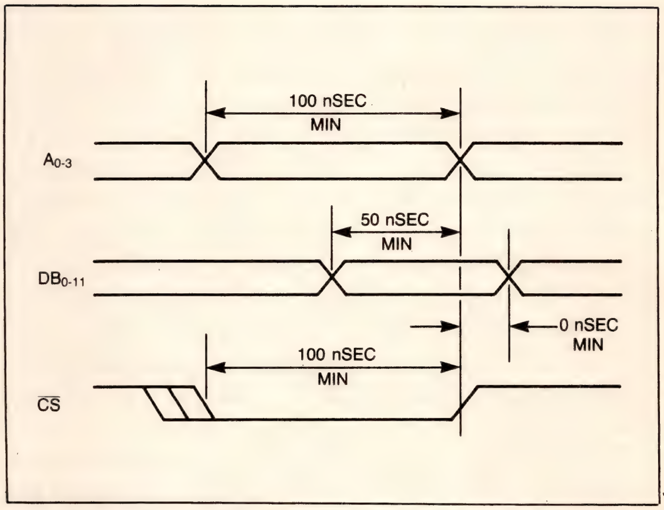


***Fig 2—A 100-nsec pulse is long enough** to select the AD667. The address lines must hold a valid address throughout the chip-select pulse, but data need only be valid during the last 50 nsec. Loading takes place on the trailing edge.*

city at each resolution. Moreover, volume controls compensate for gain errors, and ac coupling blocks the dc component of the signal, making offset errors unimportant. You can, therefore, ignore the temperature stability of these parameters. Thus, converters optimized for digital audio are often unsuitable for instrumentation and industrial applications.

Other applications require better accuracy than resolution. Consider, for example, a 1-bit D/A converter such as an electronic switch. A converter specified with ±½ LSB of total unadjusted error (a common specification for high-resolution converters) can exhibit equal outputs for two adjacent codes, because the lower code might be ½ LSB high and the upper code might be ½ LSB low. In the case of the switch, therefore, the output would remain at half the full value, regardless of whether the switch were on or off.

Closed-loop control systems can tolerate moderate nonlinearity, but they demand monotonicity to avoid feedback and oscillation. In such systems, a D/A converter with 16-bit resolution but with monotonicity guaranteed to only 14 bits is effectively a 14-bit converter. Open-loop systems, on the other hand, can sacrifice monotonicity, but they demand good relative accuracy (linearity). Further, open-loop systems that have no user trims may also require low offset and gain errors, whereas closed-loop systems can tolerate such errors.

Finally, a D/A converter's dynamic performance is also critical. The analog output must settle within a specified percentage (usually ±½ LSB) of its final value within a period determined by the application. You should be able to find the settling time for the worst-case transition in the part's data sheet.

Current-output devices usually offer faster settling times than do voltage-output devices, because current-output devices simply steer currents into a zero-voltage node (usually a virtual ground when the device is on and a real ground when the device is off). Voltage-output devices usually consist of current-output D/A converters with output amplifiers that perform current-to-voltage translation. Each amplifier adds its own settling time to that of the associated converter, so voltage-output devices have a longer settling time than do current-output devices.

*You can use a D/A converter to synthesize a waveform of almost any shape from linear segments.*

upper address for the card slot, and you can use the $\phi1$ signal to provide a write strobe. As long as no other devices use the same card slot as the AD667, you can generate $\overline{CS}$ by gating together only $\overline{DEV\ SEL}$ and $\phi1$. If other addresses are in use, however, you should also combine address lines $A_1$ to $A_3$ with $\overline{DEV\ SEL}$ and $\phi1$.

In the IBM PC, you can assign I/O ports either to the memory address space or to the separate I/O address space, depending on which write signal you select. **Fig 4** shows how to place the AD667 in the I/O space by using IOW to generate the write strobe. Ports in the I/O space need only decode the lower 10 address lines ($A_0$ to $A_9$), but the decoding logic must also accept the AEN signal to mask out DMA cycles that use the same address space.

In the circuits in both (**Figs 3** and **4**), address line $A_0$ is applied directly to the AD667's $A_1$ and $A_2$ inputs and inverted to the $A_0$ and $A_3$ inputs. The effect of these connections is that a write operation with address line $A_0$ low loads the eight MSBs of the AD667's first-rank buffer. A subsequent write operation, with $A_0$ high, first loads the four LSBs of the first-rank buffer and then transfers the entire 12-bit word into the active buffer, thereby completing the update operation and initiating the conversion of the new data.

You can write programs in any language to manipulate the D/A converter. For instance, if your application demands a high conversion rate, you may need to write your programs in assembly language. If you need to interact extensively with the program, you'll probably want to use a high-level language such as Pascal, C, or Basic. And, of course, you can combine the two techniques by writing the interactive portion of the program in a high-level language and calling a machine-language subroutine to process the data that the operator supplies.

**Use your PC as a waveform generator**

By adding a D/A converter to the Apple II and using the Basic program in **Listing 1**, you can generate waveforms of almost any shape. The program in **Listing 1** prompts you for parameters specifying a waveshape, and then calls a machine-language subroutine to generate the waveform. The maximum frequency depends largely on the number of points you specify to define the waveform; the upper limit is a function of the Apple's maximum I/O-update rate. For example, you can define a square wave with only two points and

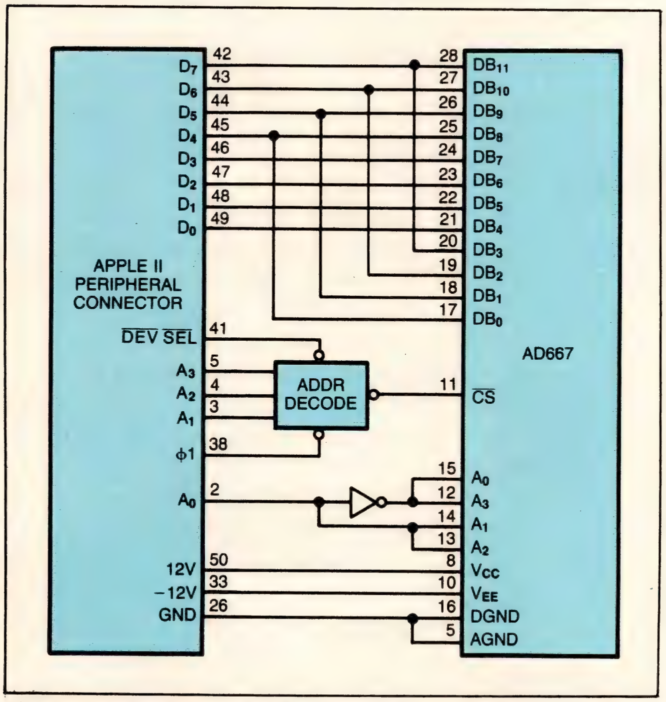


***Fig 3—You don't need much additional circuitry** to interface an AD667 to an Apple II computer, in which all I/O is memory-mapped. Address logic examines only five lines; the system clock provides a write strobe.*

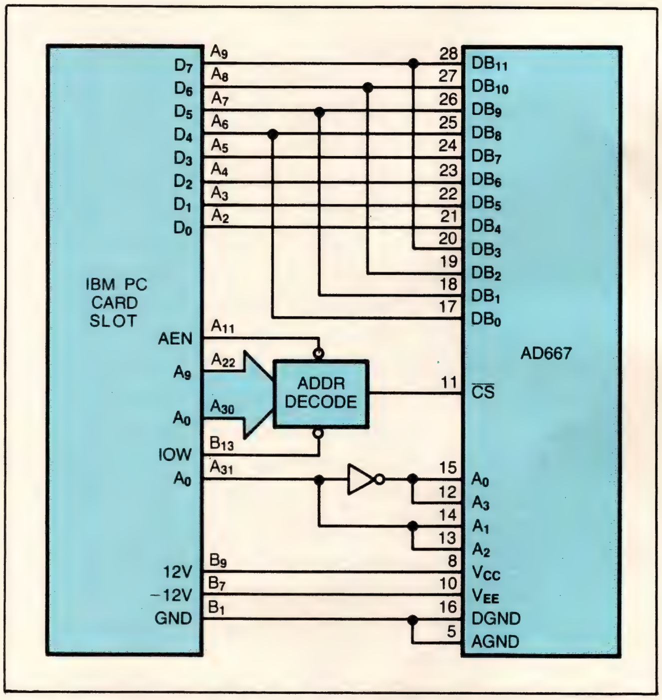


***Fig 4—Because the IBM PC has a separate address space for I/O,** when you interface the AD667 to the PC you need to decode only 10 of the 16 address lines. However, you must use the AEN signal to prevent DMA cycles from addressing the D/A converter.*

**LISTING–1**

```
10   INPUT "WHAT FREQUENCY (KHZ)?";F: PRINT
20   P = INT (31.03/F)
30   AD = 0: BD = 1
40   PRINT "MAXIMUM NUMBER OF DATA POINTS = ";P
50   IF P > 256 THEN GOTO 120
60   AF = INT (1024 * 1000 / (P * (33 + 5 * AD))) / 1000
70   BF = INT (1024 * 1000 / (P * (33 + 5 * BD))) / 1000
80   PRINT "WITH ";P; "DATA POINTS, CHOOSE BETWEEN A ";AF;"KHZ
     OUTPUT OR A ";BF;"KHZ OUTPUT.  OR CHOOSE A DIFFERENT NUMBER
     OF DATA POINTS.": PRINT
90   PRINT "DO YOU WANT ONE OF THE ABOVE FREQUENCIES (Y/N)?"
100 PRINT: GET A$
110 IF A$ = "Y" THEN GOTO 160
120 INPUT "HOW MANY DATA POINTS DO YOU WANT (1-256)?";P
130 D = 204.8 / F / P - 6.6
140 BD = INT (D): AD = BD + 1
150 GOTO 60
160 PRINT "WHICH ONE (A,B)?": GET B$
170 IF B$ = "A" THEN POKE -61695,AD + 1
180 IF B$ = "B" THEN POKE -61695,BD + 1
190 POKE -61696,256 - P
200 PRINT "THE ";P;" DATA POINTS WILL COMPRISE A NUMBER OF LINEAR
    SEGMENTS WHICH WILL FORM ONE CYCLE OF THE WAVE.": PRINT
210 INPUT "ENTER YOUR FIRST DATA POINT (0-4095)";AY
220 AMEM = -61952 - P: EN = 0
230 MSBS = INT (AY/16): LSBS = 16 * INT (AY - MSBS * 16)
240 POKE AMEM,MSBS: POKE AMEM + 256,LSBS
250 ZY = AY
260 PRINT "REMEMBER: FIRST SEGMENT DOESN'T INCLUDE THAT POINT"
270 LT = P - 1: S = 0
280 S = S + 1: PRINT
290 PRINT " HOW MANY POINTS IN SEGMENT #";S: INPUT L: PRINT
300 IF L > LT THEN GOTO 290
310 LT = LT - L
320 IF LT > 0 THEN GOTO 350
330 BY = ZY: EN = 1
340 GOTO 370
350 INPUT "ENTER VALUE OF SEGMENT ENDPOINT (0-4095)";BY: PRINT
360 PRINT "THERE ARE ";LT:" DATA POINTS LEFT."
370 FOR X = 1 TO L
380 DP = AY + (BY - AY) * X/(L +EN) + 0.5
390 MSBS = INT (DP/16): LSBS = 16 * INT (DP - MSBS * 16)
400 AMEM = AMEM + 1
410 POKE AMEM,MSBS: POKE AMEM + 256,LSBS
420 NEXT X
430 AY = BY
440 IF LT > 0 THEN GOTO 280
450 PRINT "WAVEFORM ENTRY IS FINISHED."
460 PRINT "CALL THE ASSEMBLY ROUTINE AT LOCATION 1000 TO BEGIN
    WAVEFORM GENERATION."
470 END

1000      AE 00 0F      LDX   $0F00
1003      AC 01 0F      LDY   $0F01
1006      88            DEY
1007      D0 FD         BNE   $1006
1009      BD 00 0D      LDA   $0D00,X
100C      8D DD C0      STA   $C0DD
100F      BD 00 0E      LDA   $0E00,X
1012      8D DE C0      STA   $C0DE
1015      E8            INX
1016      F0 E8         BEQ   $1000
1018      EA            NOP
1019      4C 03 10      JMP   $1003
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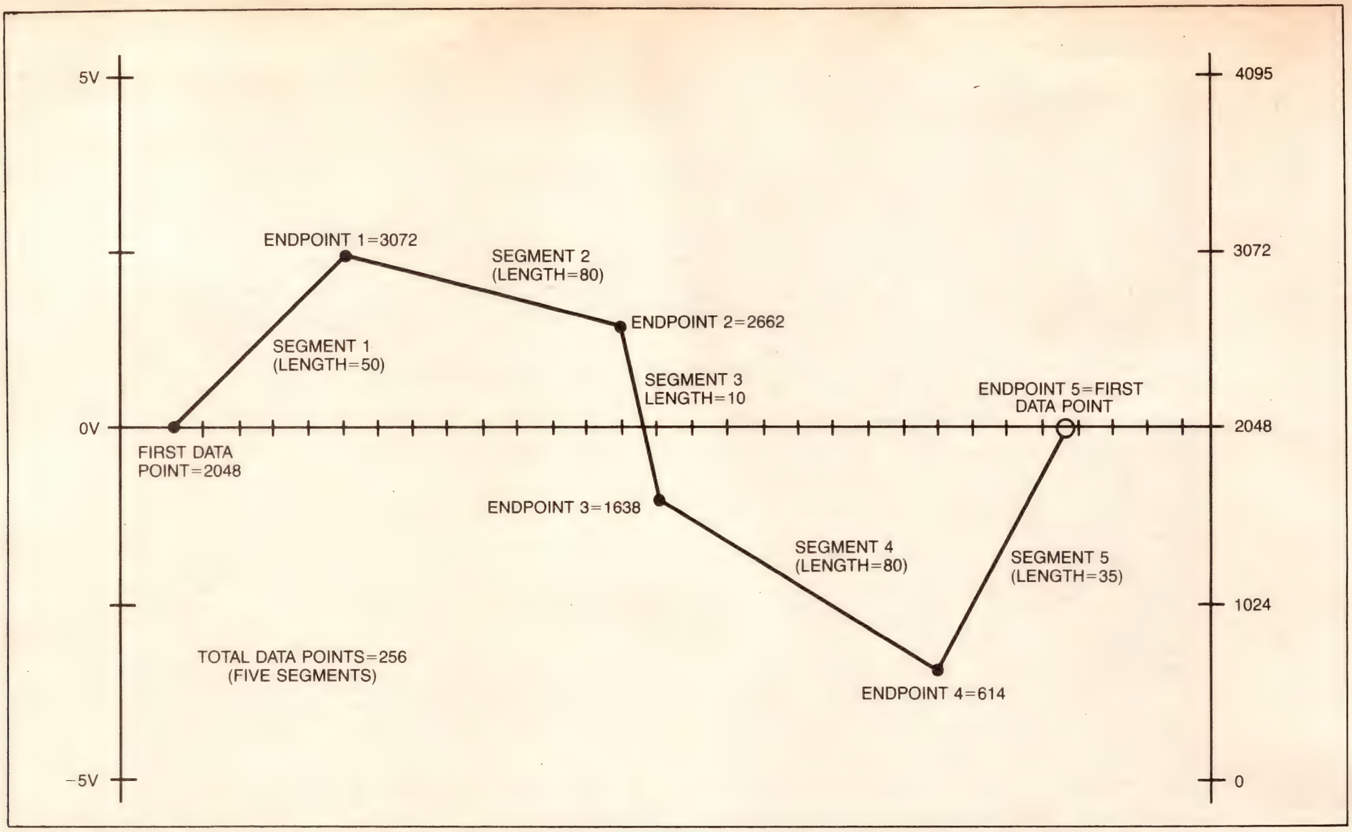


***Fig 5—You can use a D/A converter to generate waveforms** of almost any shape by specifying the beginning and end values of linear segments. The software driving the D/A converter computes the intermediate values and sends them to the converter.*

display it at frequencies as high as 15.5 kHz. On the other hand, if you use the maximum number of points (256) to define a waveshape, the maximum frequency will be 120 Hz.

Lines 10 to 90 of the program allow you to select the desired frequency and the number of points needed to define the waveform. The Apple may not be able to produce a waveform with the desired number of points at exactly the desired frequency; in that case, the program displays the two closest frequencies that are possible (one above, the other below the desired frequency) and asks you to choose one of these, or to select a different number of points.

Lines 200 to 460 prompt you to define one cycle of the waveform as a number of linear segments, each having a particular voltage value. If you configure the AD667 for a bipolar range of ±5V, these values can range from 0 (representing −5V) through 2048 (representing 0V) to 4095 (representing +4.9976V, which is full scale minus 1 LSB). Segments are specified by their length and the values of their endpoints; the end of the first segment becomes the beginning of the second, and so forth.

The program provides you with a running total of the number of data points still available to you. You indicate the last segment by assigning it all of the remaining data points; the program automatically uses the first data point you entered as the final segment's endpoint, thereby generating a continuous waveform **(Fig 5)**.

Note that lines 230 and 390 break the data-point values into left-justified binary bytes (the eight MSBs in one byte, and the four LSBs, followed by four zeros, in another byte). Lines 240 and 410 store these bytes at memory addresses that are 256 locations apart, placing the low-order byte in the higher address. As each segment's length and endpoint are entered, the loop in lines 370 to 420 calculates the value of each data point along the segment and stores these values in memory.

The calculation in line 380 uses the variable AY as the segment's starting point and the variable BY as its endpoint. In all segments except the last, the variable EN has a value of zero. To define the last segment, you assign all remaining data points to it. Line 330 then sets the segment's endpoint equal to the first data point entered, and it sets variable EN to 1. Variable EN extends the length of the segment by 1 to account for the addition of the first data point to the end of the last segment.

You can modify the program to allow the insertion of segments of sines, cosines, or other functions into the waveform. Instead of interpolating linearly between points, the program can insert a specified number of cycles of a particular amplitude of waveform that the Apple calculates. The program stores two other pieces of information required by the machine-language generation and display subroutine. The first of these, the delay needed between updates of the converter, is calculated in line 130 from the number of data points and the desired frequency. The other is a pointer (calculated in line 190) that tells the subroutine how many data points are stored.

The machine-language subroutine uses register X to

*By adding D/A and A/D converters and some interface circuitry to your PC, you can apply known voltages to a device and measure the device's response.*

keep track of the current memory address in the data-point space, and it uses register Y to hold the delay value. The subroutine continually scans the memory space containing the data points and resets when incrementing register X results in overflow. Using indexed addressing, the subroutine fetches the MSB and LSB for each data point (lines 1009 and 100F, respectively) and sends the values to the AD667, which is located in addresses C0DD$_{HEX}$ and C0DE$_{HEX}$. As soon as an update of the converter is complete, the program reloads the delay value into register Y and counts up from zero. When the count equals the delay value, the BNE instruction in line 1009 terminates the delay.

The speed of the computer's processor determines the upper frequency limit of the system. You could operate at higher frequencies by arranging for a DMA controller to fetch data points directly from memory without processor intervention. However, you'd also have to modify the Basic program to fill the delay time either with duplicates of the previous data point or with more interpolations.

Besides using your PC to generate waveforms, you can use it to test analog ICs. By using both D/A and A/D converters, you can program your PC to apply a test voltage to an analog IC and also to monitor the outputs of the IC under test to see if they're within acceptable limits.

For example, you can build a circuit for testing 10V

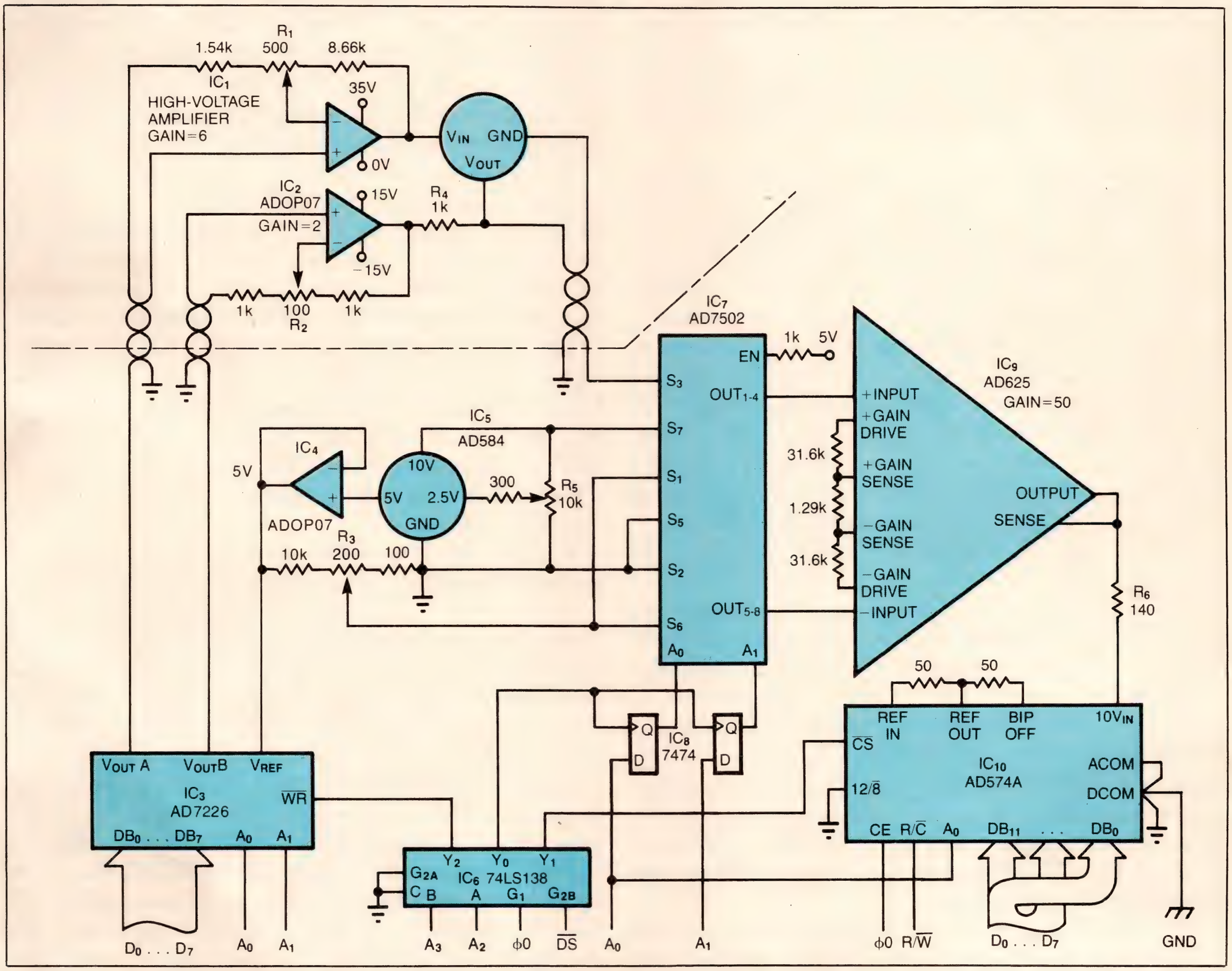


***Fig 6—You can test voltage-reference ICs** with this circuit. The digital interface is for an Apple II computer, but you could easily modify it to suit an IBM PC.*

*To measure a signal as an offset instead of an absolute voltage, include a differential amplifier in your test circuitry.*

voltage-reference ICs, power supply regulators, and similar components. **Fig 6** shows the necessary circuitry for testing the AD581, a 10V voltage-reference IC. The test circuitry consists of two parts: the interface board equipped with D/A and A/D converters, and a remote test fixture containing two op amps and a socket for the device under test (DUT). The digital interface shown is configured for an Apple II; however, you could easily modify the interface to suit any other PC.

On the computer interface board, a quad 8-bit D/A converter (the AD7226, which is similar to the AD667) generates two analog output signals that are variable from 0 to 5V and passes them to the remote test fixture. One of these control signals, amplified by $IC_1$, which has a gain of 6, applies a line voltage between 0 and 30V to the DUT's input terminal. The other control signal, amplified by $IC_2$, which has a gain of 2, determines the voltage across resistor $R_1$ and thereby varies the load current drawn from the DUT between 0 and 10 mA.

The voltage output of the DUT is applied, through CMOS multiplexer $IC_7$ and buffer amplifier $IC_9$, to A/D converter $IC_{10}$. The AD7502 CMOS multiplexer and AD625 buffer amplifier also provide a self-calibration feature. One differential channel ($S_6$) of the AD7502 carries an accurate 100-mV reference voltage that's derived, via resistor $R_3$, from the buffered 5V output of the AD584 reference source. A second channel ($S_1$) carries the same 100-mV reference with inverted polarity. The third channel ($S_3$) carries the DUT's output signal, which is referred to the AD584's 10V output. The output of the AD7502 multiplexer, amplified by a factor of 50 in the AD625 differential amplifier, is applied to the input terminal of the AD574A A/D converter.

The program you use to calibrate the DUT must begin by causing the multiplexer to select the −100-mV reference voltage. Multiplied by 50, this reference voltage will appear at the input of the A/D converter as −5V plus some offset and gain errors induced by the AD625 amplifier and the resistor tolerances in the associated gain-setting network. Because this signal will be close to negative full scale, you can ignore the effect of any gain errors and store the difference between the AD574A's measurement and the ideal code of 000H as the system offset.

Next, your program must select and measure the 100-mV reference signal. The software should then subtract the system offset from the AD574A's measurement and calculate a system gain correction factor. These gain and offset figures are intentionally inflated: Resistor $R_6$ expands the A/D input range to ensure that the 100-mV and −100-mV measurements fall within the A/D converter's input range, even with worst-case system errors. During the test, the program should correct each measurement of the DUT's output voltage by subtracting the system offset and multiplying the result by the gain-correction factor. The accuracy of the measurement thus depends only upon the accuracy of the reference voltages.

Because the differential multiplexer output is the difference between the DUT's output and the AD584's 10V reference, calibration errors appear as offsets, which you must null by adjusting resistor $R_5$. Likewise, calibration errors in the 100-mV references appear as gain offsets; you must null these, too, by adjusting resistor $R_3$. If, as in the ideal case, these errors were reduced to zero, the accuracy of the measurement of the DUT's output voltage would be limited only by the A/D converter's resolution and linearity.

A drawback of this scheme, as with any software testing scheme, is that it may degrade the system's resolution. Remember that you have to expand the converter's input range to a degree that allows it to handle worst-case system errors. Only a portion of the 4096 possible output codes (12-bit resolution) are usable in the test, therefore, so resolution over the whole signal range is degraded. In the circuit in **Fig 6,** however, even if system errors were so extreme that only half the input range could be used for device testing, resolution would still be no worse than 50 μV/LSB, which is well below the noise threshold inside the PC's case.

You can use the Basic program in **Listing 2** to perform the entire test procedure. The program, which is written for an Apple II computer, begins by prompting you to enter the appropriate line and load conditions for the DUT. It sets the control signals accordingly by writing these values to the 8-bit AD7226 D/A converter, which offers 120-mV resolution for the line voltage and 20-μA resolution for the load current.

Because adjusting the voltage across resistor $R_4$ sets the load current, the calculation in line 90 of the program must assume that the DUT's output voltage is 10.000V. Any deviation from this value will induce an error in the load-current condition. If you wish to set the load current more accurately, you can modify the program: First you'd set the load current using the assumed value, and then you'd measure the DUT's error and reset the load current using the measured

*Programs for automated test equipment should measure and compensate for system errors such as offset and gain.*

value. This recalculation would be similar to the one in line 90, except that you'd substitute the measured output value for the assumed value.

Once the test conditions are set, the program measures the system offset and gain errors by writing the appropriate multiplexer address and then using the Poke statement to put a zero into the lower address, triggering A/D conversion. You select the −100-mV channel, and line 160 calculates offset as the deviation from the ideal 000H. Then you select the 100-mV channel, and line 200 calculates gain error as the deviation from the ideal code of 4095.

If system errors are so gross that they fall outside the expanded input range of the converter, the program displays an error message. Line 270 selects the DUT output and triggers conversion; line 290 calculates the offset from the ideal 10.000V.

The test circuitry can measure DUT errors as large as ±100 mV. However, if the DUT error, combined with system offset and gain errors, falls outside the converter's expanded input range, the program displays an overrange error message. If the DUT error,

**LISTING—2**

```
10  PRINT "SET LINE VOLTAGE"
20  PRINT "AD581 IS SPEC'D FROM 13-30V"
30  INPUT "WHAT INPUT VOLTAGE (V)?";VOLT
40  DOUTA = INT (VOLT * 256/30.117 + 0.5)
50  POKE -16168,DOUTA
60  PRINT "SET LOAD CURRENT"
70  PRINT "AD581 IS SPEC'D FROM 0-5MA"
80  INPUT "WHAT LOAD CURRENT (MA)?";LOA
90  DOUTB = INT (256 * 10.000/10.039 - LOA * 256/10.039 + 0.5)
100 POKE -16167,DOUTB
110 REM
120 REM    MEASURE SYSTEM OFFSET AND GAIN ERRORS
130 REM
140 POKE -16175,0: POKE -16172,0
150 INHIGH = PEEK (-16172) * 16
160 OFFSET = INHIGH + PEEK (-16171)/16
170 IF OFFSET = 0 THEN PRINT "GROSS SYSTEM ERROR LOW"
180 POKE -16176,0: POKE -16172,0
190 INHIGH = PEEK (-16172) * 16
200 GAINERR = INHIGH + PEEK (-16171)/16
210 IF GAINERR = 4095 THEN PRINT "GROSS SYSTEM ERROR HIGH"
220 GAINERR = GAINERR - OFFSET
230 GAINADJ = 2 - GAINERR/4095
240 REM
250 REM    MEASURE AD581'S OUTPUT VOLTAGE
260 REM
270 POKE -16174,0: POKE -16172,0
280 INHIGH = PEEK (-16172) * 16
290 MEAS = INHIGH + PEEK (-16171)/16
300 IF MEAS = 0 THEN PRINT "GROSS DEVICE ERROR LOW"
310 IF MEAS = 4095 THEN PRINT "GROSS DEVICE ERROR HIGH"
320 ERR = (MEAS - OFFSET) * GAINADJ
330 REM
340 REM    SCALE ERROR TO MV AND PRINT
350 REM
360 ERR = INT (MEAS * 200 / 4095 - 99.5)
370 PRINT "AD581'S OUTPUT VOLTAGE ERROR IS ";ERR;"MV"
```

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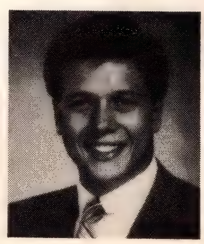
after being corrected for system offset and gain errors, is within range, the program scales it to millivolts and displays it.

### Calibrate the control voltages

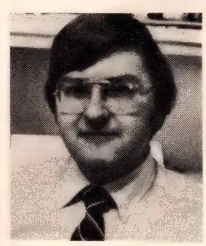
When you use the test circuitry, you must periodically calibrate the line and load test conditions by adjusting the gain of the amplifiers on the remote test fixture. To calibrate the line voltage, you enter a request for a 30V line voltage and adjust resistor $R_1$ until the output of amplifier $IC_1$ is exactly 30V. The D/A converter's highest output is 1 LSB below full scale, so full-scale voltage is 30.117V (this full-scale-voltage value is used in the calculation of line 40.)

To calibrate the load current, you enter a request for 0V (which sets the D/A converter to full scale), and you adjust resistor $R_2$ until the output of amplifier $IC_2$ is exactly 10.000V. Full-scale voltage is 10.039V; this value appears in the calculation in line 90. If you're going to set load current using the DUT's measured output voltage, however, you'll need to adjust resistor $R_2$ for an amplifier output voltage of 10.100V to accommodate worst-case DUT errors. In this case, full-scale voltage will be 10.139V, so you'll have to substitute this value for the full-scale value (10.039V) in line 90 of the program. **EDN**

## Authors' biographies



*John Croteau was a product marketing engineer at Analog Devices (Wilmington, MA) when he coauthored this article. He provided marketing support for bipolar data converters. He is currently employed by Crystal Semiconductor (Austin, TX). John holds a BS in Engineering Science from Penn State University and is a member of the IEEE.*



*Doug Grant is the new-product marketing manager at Analog Devices (Wilmington, MA), where he is responsible for defining new data-converter products. Doug, who holds a BSEE from the University of Lowell, has been with the company for nine years. In his spare time, Doug collects antique radio and electronics books. He holds an amateur radio license.*

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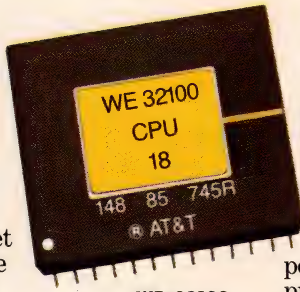


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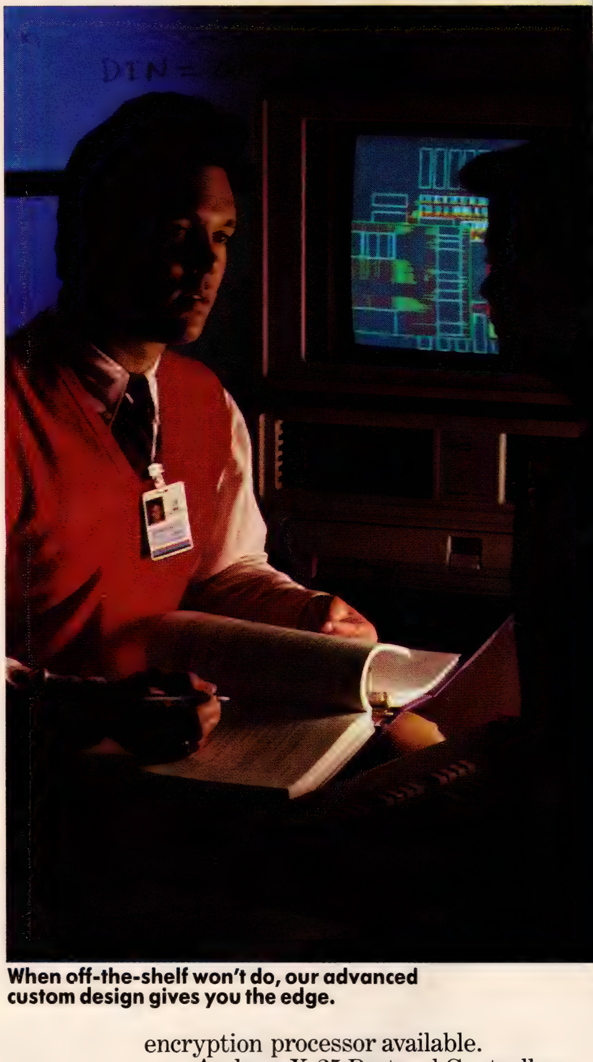

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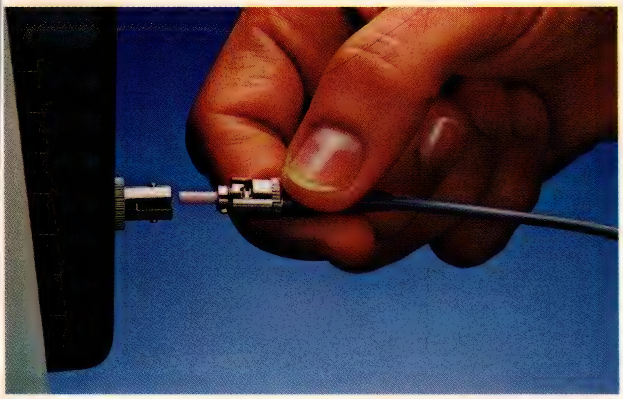

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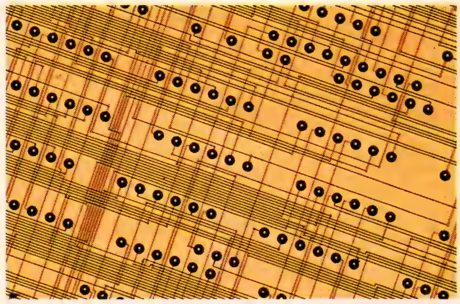

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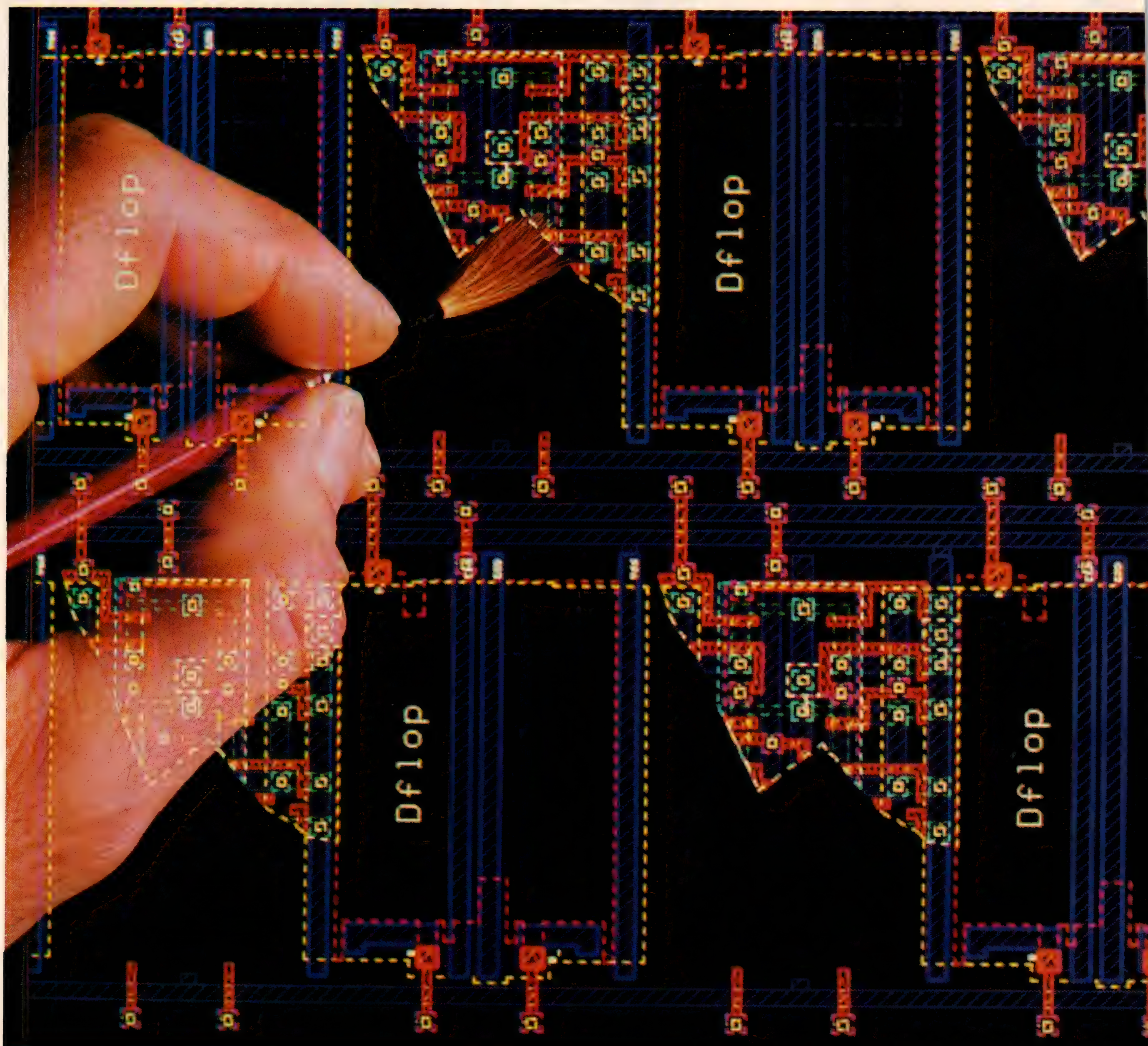

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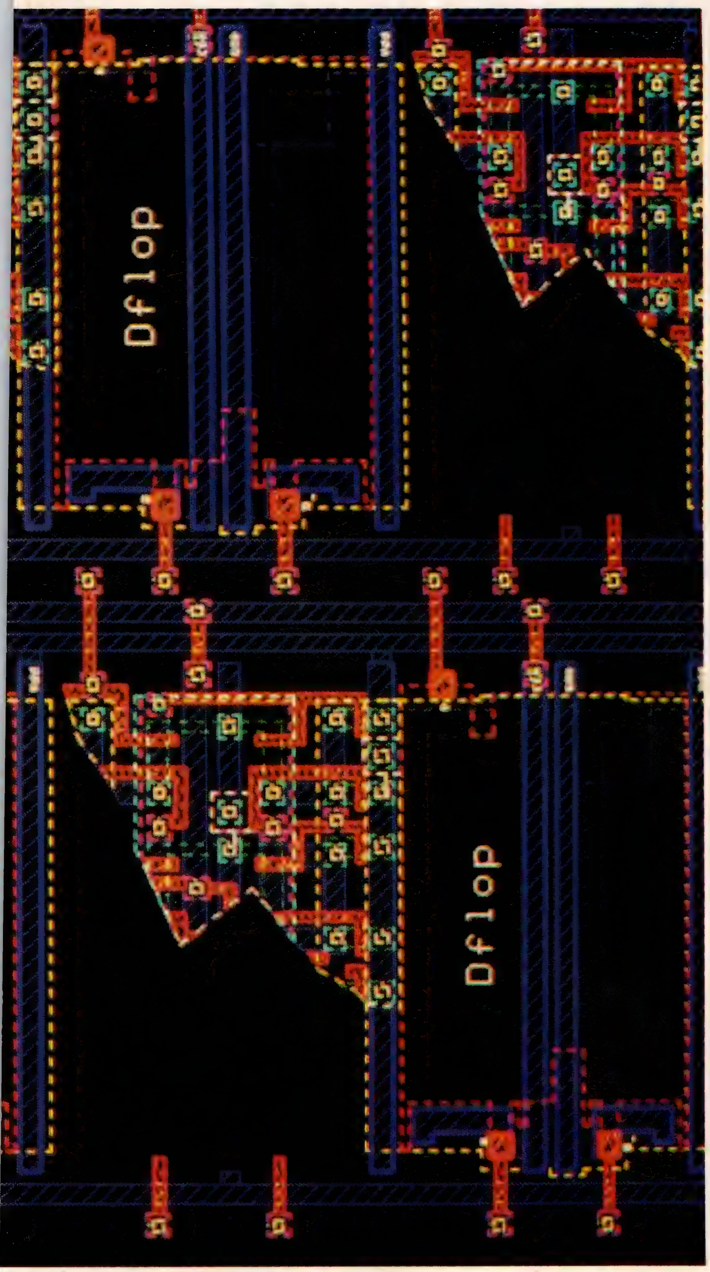


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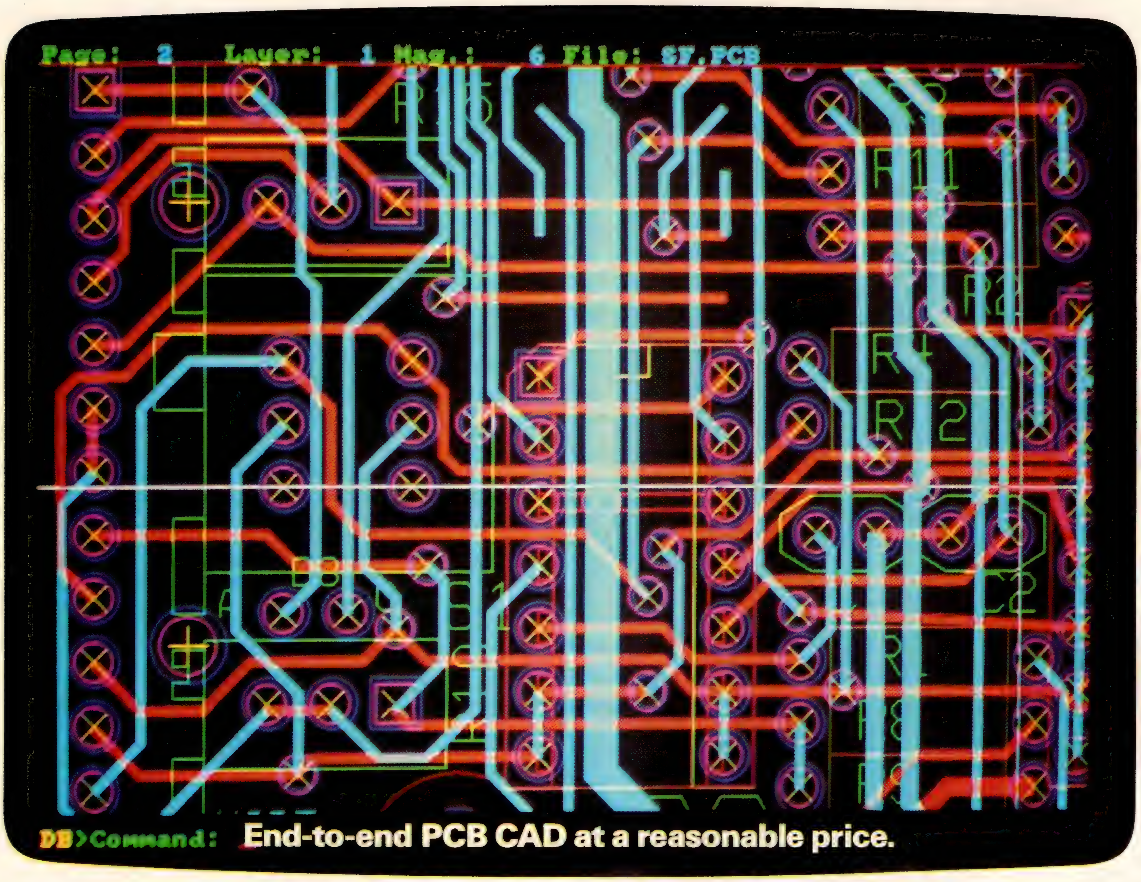


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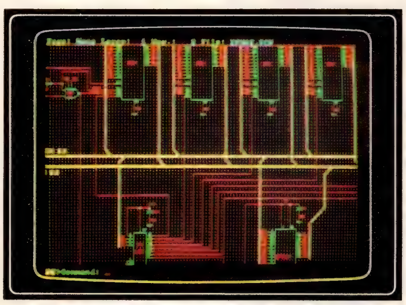

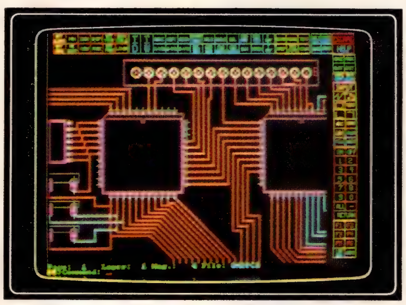

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# Methodology speeds VLSI circuit design cycles

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Albert Feller, *RCA Corp*

Given the complexity of today's application-specific integrated circuits, chip designers can't help but encounter excessively long design cycles using conventional layout methodologies—methodologies based on past LSI or even MSI design approaches. A new methodology, using current design aids and tools, reduces the design time of custom LSI and VLSI devices with 30,000 transistors or more by at least 50%. It achieves this reduction with little loss in performance, and it exacts an area premium of only 5 to 15%, depending on the ratio of functional to random logic.

The methodology is based on an automatic placement and routing capability and works in conjunction with additional supporting tools (see **box,** "A look at the design system"). Most important, it performs virtually all of the basic VLSI design tasks in parallel, as opposed to the sequential, or coincidental, mode that characterizes the conventional design methodologies; the schedule for generating a validated layout is generally independent of the chip layout.

Before addressing the question of layout technique, it's important to clarify one point: Don't confuse design methodology with design tools. For example, standard cells, handcrafted design, macrocells, automatic placement, and automatic routing are design tools, not design methodologies. Similarly, programs like logic simulators, design-rule checkers, logic validation, and circuit analysis are design aids, not design methodologies. A design methodology defines procedures and establishes guidelines for utilizing design aids and design tools to delineate and lay out VLSI devices.

Virtually all design methodologies contain the following tasks: partitioning and preliminary logic design, initial macrocell definition (RAM, ROM, register stack, multiplier, bit slice, ALU, etc), macrocell design and validation, logic design, logic simulation, (including generation of test vectors), chip layout, and fault simulation.

*Text continued on pg 154*

## A look at the design system

Encompassed in a self-contained turnkey system, the RCA VLSI design system (**Fig A**) operates on just about any virtual-memory computer that has a Fortran compiler. The system contains a technology file of standard-cell and gate-array-cell families, a set of CAD VLSI design tools, and an operating system that relieves the user of all tasks except the submission of the input logic and a corresponding set of test vectors.

The system's CAD tools include the following: MP2D, a standard-cell and macrocell automatic layout program; Autodelay, a timing-analysis program; Criptic, a critical-path analysis program; Enlave, an automatic design-rule and logic-verification program; and Mimic, a multiple, hierarchical logic-gate and fault-simulator program.

MP2D is the key program that made possible the development and implementation of the new design methodology. Originally developed during 1971-1972, it has undergone numerous enhancements and improvements. From 1971 to about 1981, MP2D's development focused on fully automatic placement of cell primitives using a parameterized algorithm as well as an automatic router based on a direct and channel-router algorithm. Over the last five years, development emphasis has shifted to automatic partitioning that provides grouping and clustering capability, and the quasi and physical placement of large blocks of logic such as macrocells.

The Autodelay program (together with the active cell delay in the technology database) automatically extracts the resistive and capacitive parasitics and computes the delay between any node pair in the layout. Program accuracy is within 20% of any Spice calculation. However, the program requires only seconds to compute any delay. Thus, a system user can employ this program as a real-time, timing-analysis tool.

The Criptic program automatically identifies all of the combinational paths between all registers. Working with the Autodelay program, under control of the operating system, Criptic then computes the delay of each path and compares the result with a reference delay—a clock period, for example. In essence, the program automatically determines the critical path in real time. Such a capability is an absolute requirement for the design of today's high-speed VLSI devices.

The Enlave program automatically checks and verifies the topology for all the interconnections for any layout generated by the automatic layout program. This application-specific design-rule checker eliminates the need for costly design-rule checkers such as PDS and ECAD. In addition, Enlave extracts the logic connectivity from the MP2D artwork and, together with the LOGCHK program, verifies that the logic connectivity embedded in the final artwork is identical to the input logic.

The Mimic program is a multistate logic-gate simulator and fault simulator that uses a concurrent grading algorithm. It has hierarchical capabilities; ie, it can functionally simulate functions such as ROMs and PLAs.

### Chip design optimization

To start the design optimization procedure, you first enter the chip logic (in the form of a net list containing the selected standard cells and their interconnects), along with a set of test vectors, and allow the MP2D program to run in a fully automatic mode. The system will automatically supply MP2D with all the information it needs to execute a run.

Initially, the automatic partitioning algorithm will place all of the input cells into groups or bins in accordance with the logical or functional relationship that exists between the various groups. The algorithm will then place the cells in each bin into a square (domain) whose area is a function of the cells in each bin. Next, it places the domains relative to each other in accordance with the logical and functional relationship between them.

The MP2D then converts each domain area to a rectangular area in accordance with the degree of logical connectivity between the adjacent domains. Everything performed so far constitutes the domain aspect ratio and domain-placement algorithm. Essentially, the prepro-

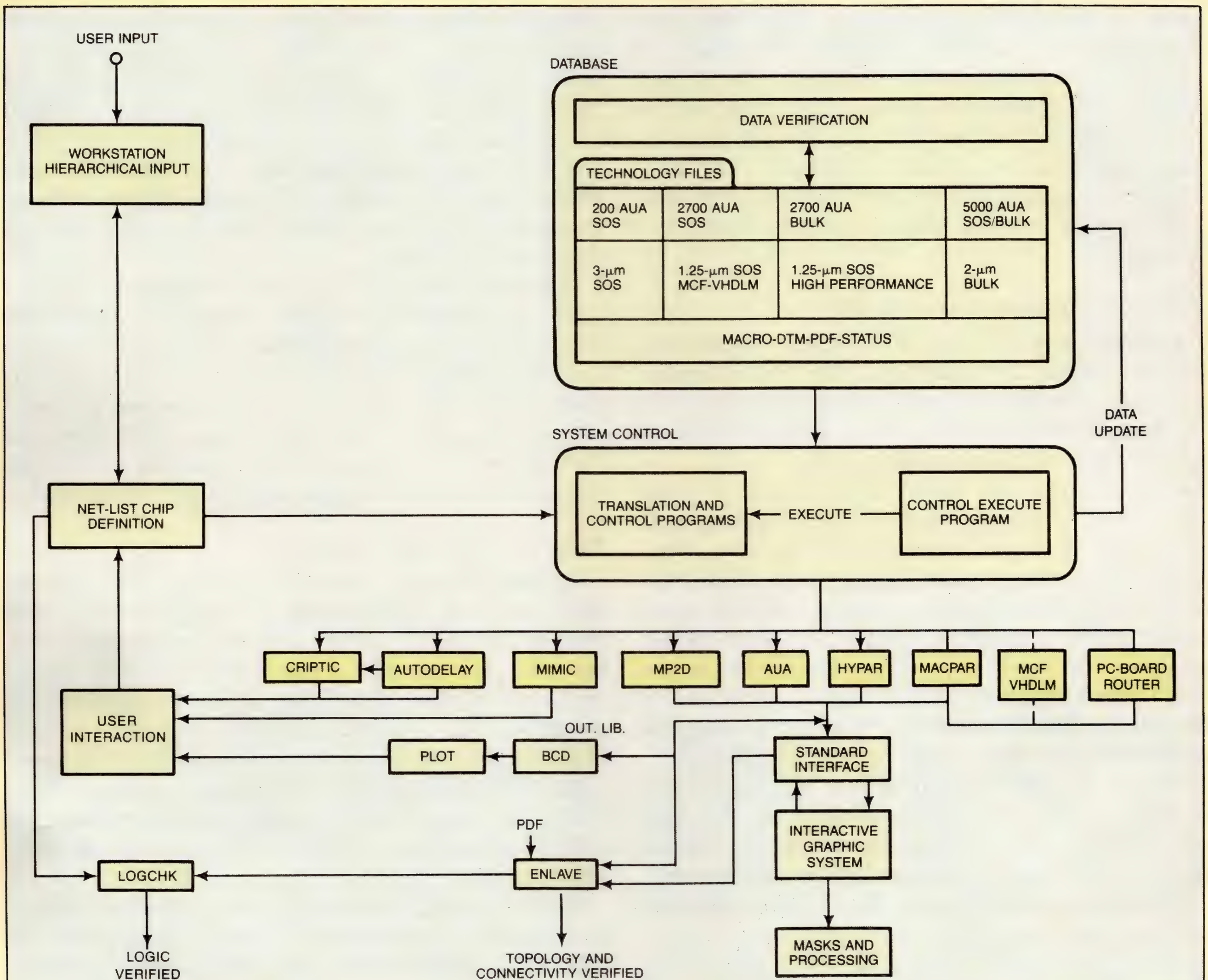



***Fig A—Operating on any virtual-memory computer*** *that has a Fortran compiler, the RCA VLSI design system contains a technology file, a complete set of design tools, and an operating system.*

cessor function is complete.

The output of the preprocessor serves as the initial-placement input for the pair-interchange cell-placement algorithms. The MP2D completes the cell-placement algorithms, and then the automatic routing algorithm guarantees 100% connectivity for each run. If you so desire, the system can generate a check plot of the final chip layout at this point. You can also initiate the area-optimization procedure now.

While reviewing the layout, you can interactively modify the placement of the domains or cells in an attempt to reduce the chip area. Time required to complete this process can range from a few minutes to one or two hours.

Next, you run the MP2D program to automatically place any unfixed cells and complete the routing function. This process will usually reduce the chip area; you can repeat the process if additional area optimization is necessary, or you need to complete some other design limitation step (logic or macrocell design, for example).

*Conventional design methodologies are to blame for excessive and unacceptable design-time cycles for ASICs.*

ASICs are chips designed for dedicated, special-purpose, or user-defined applications. Typically, it's a system designer's function to define the devices. A system designer performs chip partitioning and then generally verifies the functionality of the chip (using a high-level simulator) at the functional or register transfer language (RTL) level. After verification, the documentation (containing the functional description that includes vectors used for system simulation) goes to a chip designer.

### Performing chip design the old way

**Fig 1** illustrates how you would handle chip design using a conventional methodology. The typical elapsed times shown are for the logic design and layout of a device containing about 160,000 transistors, 35,000 of which are associated with random logic.

The first step in the overall design involves initial macrocell definition and logic design, starting from functional or hierarchial description of the chip. Typically, it's during this phase that you generate test vectors and implement logic simulation. At this point, you also usually accomplish prelayout dynamic calculations using the delay and timing capabilities of the logic-simulator design tool. Including the generation of additional functional macrocells, nine months is typical for this stage for a chip of this size and complexity.

According to conventional layout techniques, the next stage usually involves the generation of a floor plan, which attempts to place the previously defined macrocells and remaining random logic in a relationship that will facilitate the following step, routing. Generally, you define other macrocells while generating the floor plan. Because it's difficult to interconnect random logic functions on a workstation (or any system supporting interactive routing), many chip designers use functional blocks (such as programmable-logic arrays) for random-logic-function implementation. You absolutely must have an efficient and optimized floor plan to ease the routing problem, and you also must take pains to address the orientation of the I/O pins on all the macrocell functions.

You have only one way of determining whether you've generated an effective floor plan: You must implement the interconnections. By the time you've executed sufficient interconnects to evaluate the floor plan, it's often too late to generate a new one if results of the routing phase show such a step is necessary. As the requirement for higher density increases, this time-frame problem becomes proportionally more critical.

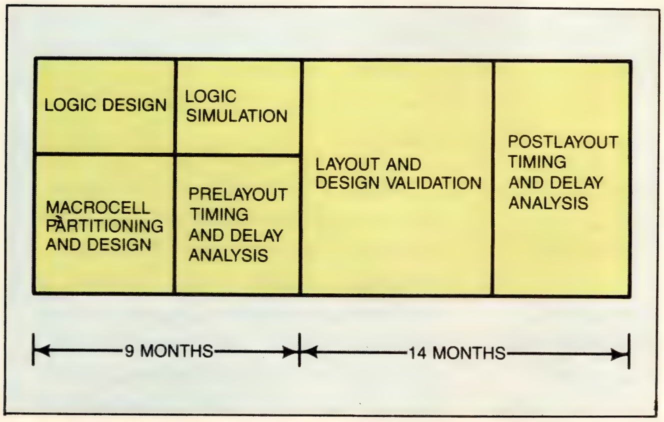



***Fig 1—Conventional custom VLSI design methodologies** dictate that you perform chip design tasks in a sequential manner. The typical elapsed times shown here are for the design of a device containing about 160,000 transistors, of which 35,000 are associated with random logic.*

### Time to verify and validate

At this point in the process, you must verify that the chip meets its performance, propagation-delay, and clock-speed specifications. You also must make sure that all race conditions and clock-skew and timing problems (if they exist) have been brought to the attention of the system designer. Generally, a logic simulator that has timing-analysis capability will serve to measure performance. For acceptable accuracy, however, the analysis must include parasitic capacitance and resistance figures to update the appropriate simulation models.

After updating the model for active load conditions, you should repeat the timing analysis, taking corrective action if dynamic performance fails to meet specification. Corrective action might involve a change of drivers, a change in the layout, editing of the interconnects and, perhaps, functional changes.

A layout validation involves a design-rule check (DRC) and verification that the logic reflected in the output layout (artwork commands) is in fact identical to the logic input from the system designer. A DRC of a conventional handcrafted layout entails the use of costly, computer-intensive programs (eg, a PDS or ECAD system). You perform output-logic verification via manual line-tracing to synthesize the logic from the traced logic—a difficult, laborious, and error-prone technique. Systems such as ECAD and PDS also have the ability to synthesize transistors and gates from the layout, thereby providing a tool to help you verify the validity of the output logic.

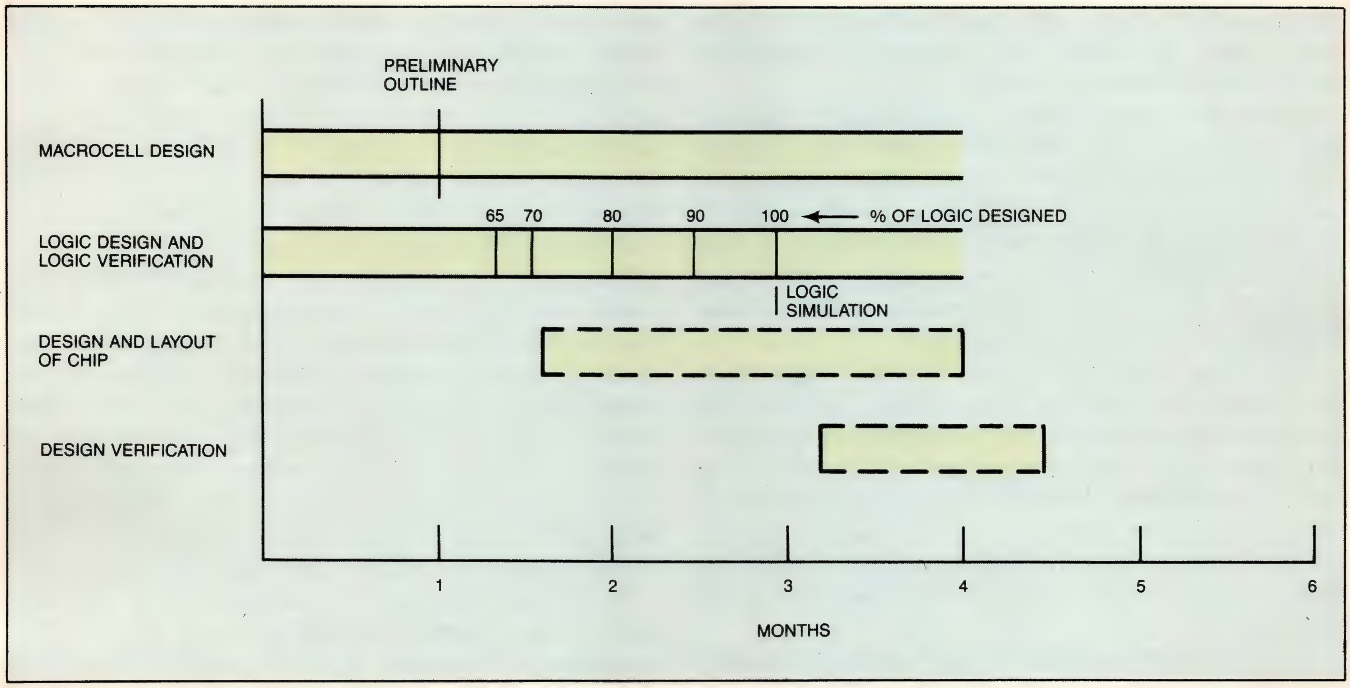



***Fig 2—Using the new design methodology,*** *you can accomplish the design and layout of the macrocell, the design and verification of the logic, and the design and layout of the chip in parallel.*

**Fig 2** illustrates the basic concept of the new design methodology. Note that the design and layout of the macrocell, the design and verification of the logic, and the chip design and layout are accomplished in parallel. Design time to complete the chip layout depends on the macrocell design or the logic design, whichever is longer. The chip layout is shown as a dashed line to emphasize that the time it takes is a variable determined by the macrocell or logic design.

Consider the design and layout of a chip, described at the functional or RTL level, that contains a functional macrocell like a RAM, ROM, register stack, multiplier, barrel shifter, etc. Because of a macrocell's functional nature, you can generally define it early in the design cycle. Early on, you can make estimates of its size, aspect ratio, and pin orientation (shown in **Fig 2** as the preliminary outline).

You initiate logic design at the start of the program. After defining about 70% of the logic (still unverified), you can generate a net list (interconnection list) and enter it into an automatic placement and routing program that proceeds to lay out the chip automatically. The logic is incomplete at this time, and thus this layout is obviously only a preliminary one. Nevertheless, you can review and optimize this layout using various support tools that are compatible with the automatic placement and routing capability. Layout optimization continues until all the logic circuitry is generated and verified. At this time, you can begin the logic-simulation and fault-grading process.

You can also initiate design verification at this point. Assuming the design and layout of the macrocell is already complete, then logic design becomes the limiting factor. Once you verify the logic, you can use special-purpose design-rule checking tools to validate the layout, and then use another program that automatically verifies the output logic.

### Consider the design of a computation chip

In order to illustrate the new design methodology in more specific terms, consider the layout of a 38,500-transistor signal-processing computation chip containing two macrocells—a 50-nsec 18×18-bit multiplier and a 16×32-bit register stack. In this case, the designer received chip specifications at a functional level, so it was essential to implement a complete, detailed logic design initially. And, because of the multiplier's operating-speed requirement, it was also necessary to develop a special optimized Booth algorithm.

Estimates indicated that the design and layout of the multiplier would exceed logic design time. Therefore, the proposed schedule for the chip **(Fig 3)** specified that

*A design methodology defines procedures and establishes guidelines for utilizing aids and tools to design and lay out VLSI devices.*

the multiplier design time would define overall chip layout time. As shown, the schedule allotted four months for the multiplier design.

It took about two months to complete and verify the logic design. In the first few weeks, the designer generated (on a preliminary basis) the multiplier outline, aspect ratio, and pin assignment. Via the automatic partitioning, placement, and routing capability of the RCA VLSI design system, it was possible to utilize the incomplete logic and the preliminary outline of the multiplier to generate a chip layout.

Employing a series of special-purpose design tools, the designer was able to coincidentally optimize the dynamic performance and the topological design of the chip layout. A dynamic-performance optimization tool, the Criptic program, identified and selected the critical timing paths automatically. Criptic extracted the parasitics associated with the interconnections and performed delay analysis that included the effect of the layout parasitics.

In parallel with the dynamic-performance evaluation and optimization, the design system utilized its automatic partitioning and placement capabilities to optimize placement (and therefore layout) topology while logic and multiplier macrocell design took place. The automatic routing program then laid out the chip. This program is really the key tool in the design methodology: It allows design functions to be done coincidentally as opposed to sequentially.

Design of the multiplier—the schedule-limiting item —did take four months to complete. Chip layout, checked for logic correctness and design rules, and mask artwork generation required an additional two weeks. Thus, a design that normally would have taken 12 to 14 months to lay out using conventional approaches took less than five months. Note that for this circuit (about half of its almost 39,000 transistors are dedicated to random logic), the final design featured an overall chip density of less than 2 $mil^2$ per device.

To further illustrate the advantages of the new methodology, consider the layout cycle for a 54,000-transistor device, part of a μP chip set. This chip

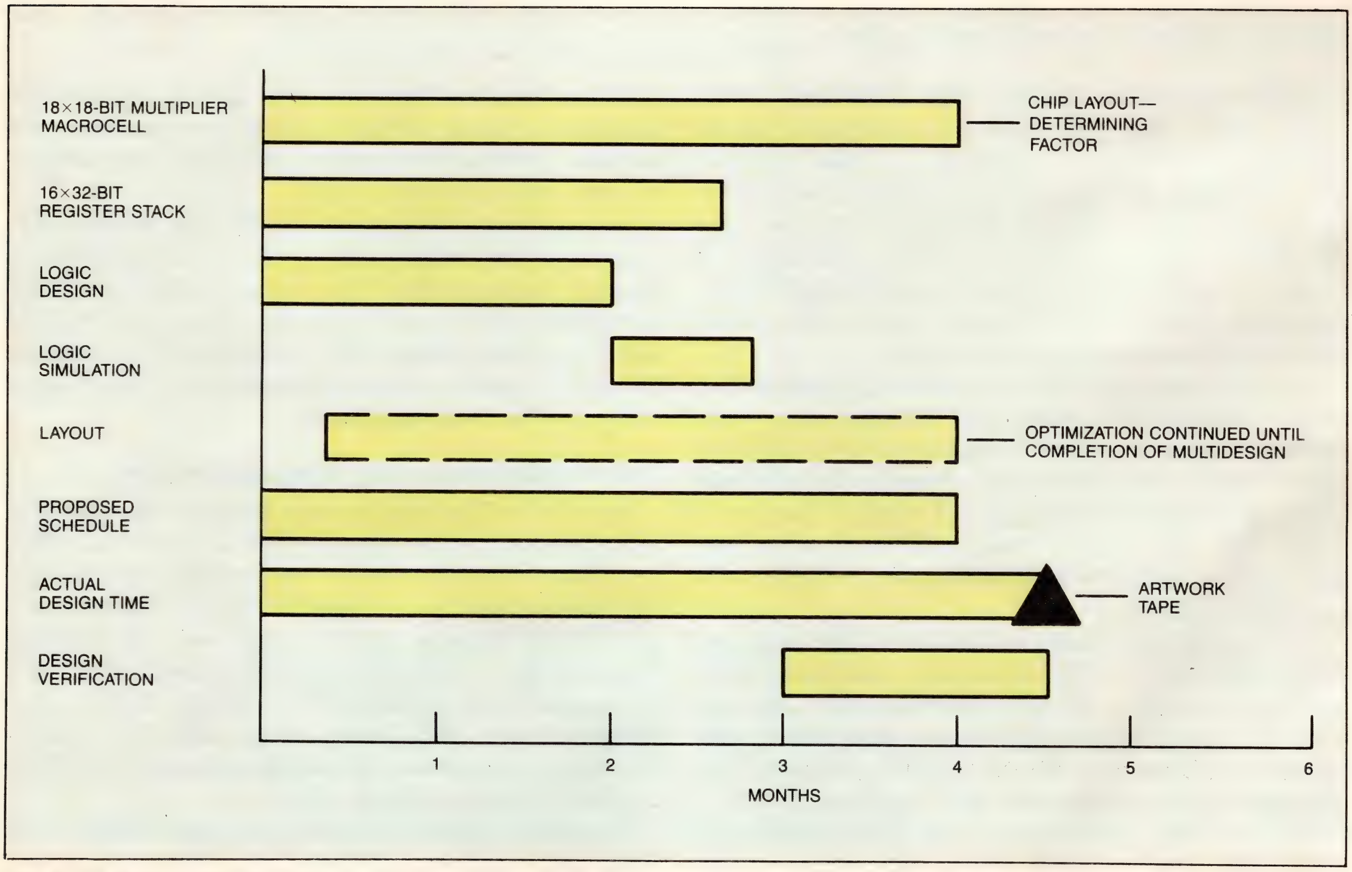
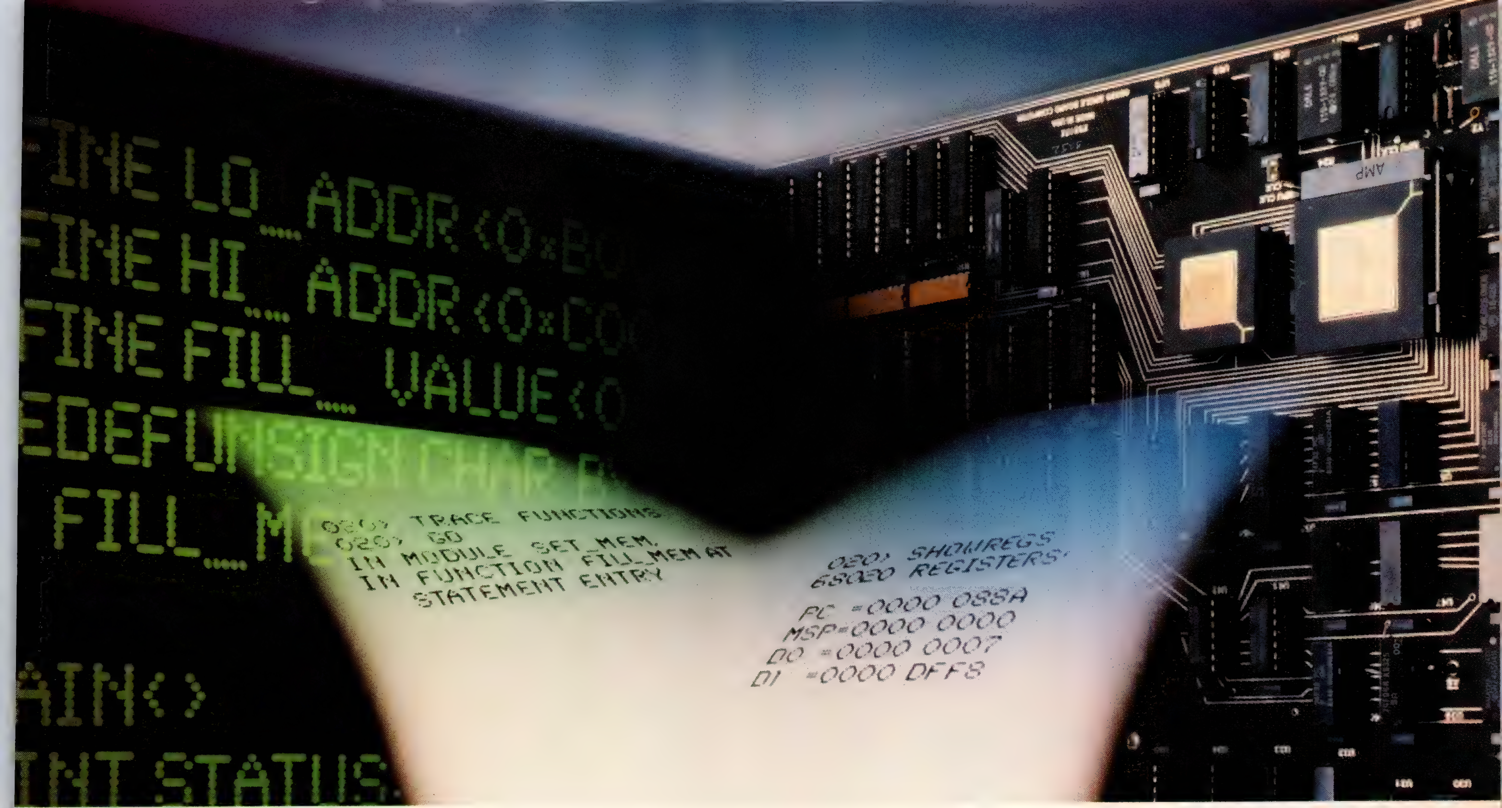



***Fig 3—In this schedule** for design and layout of a signal-processing chip, multiplier design time defines the chip layout time.*

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*The first step in the overall logic design involves initial macrocell definition and logic design, starting from functional or hierarchical description of the chip.*

contains one macrocell—a 32×32-bit register stack.

In this case, the logic design was supposedly complete but unverified (no test vectors generated). As a result, the chip designer estimated that the design, layout, and complete verification/validation process for the 32×32-bit register-stack macrocell would take about four months. This limiting factor established the original schedule **(Fig 4a)** for the entire chip design.

As it turned out, the logic design wasn't complete. It experienced at least two major changes and wasn't verified as correct until more than four months after the start of the chip design program. From a practical standpoint, logic design rather than macrocell design became the limiting factor **(Fig 4b)** for the design and

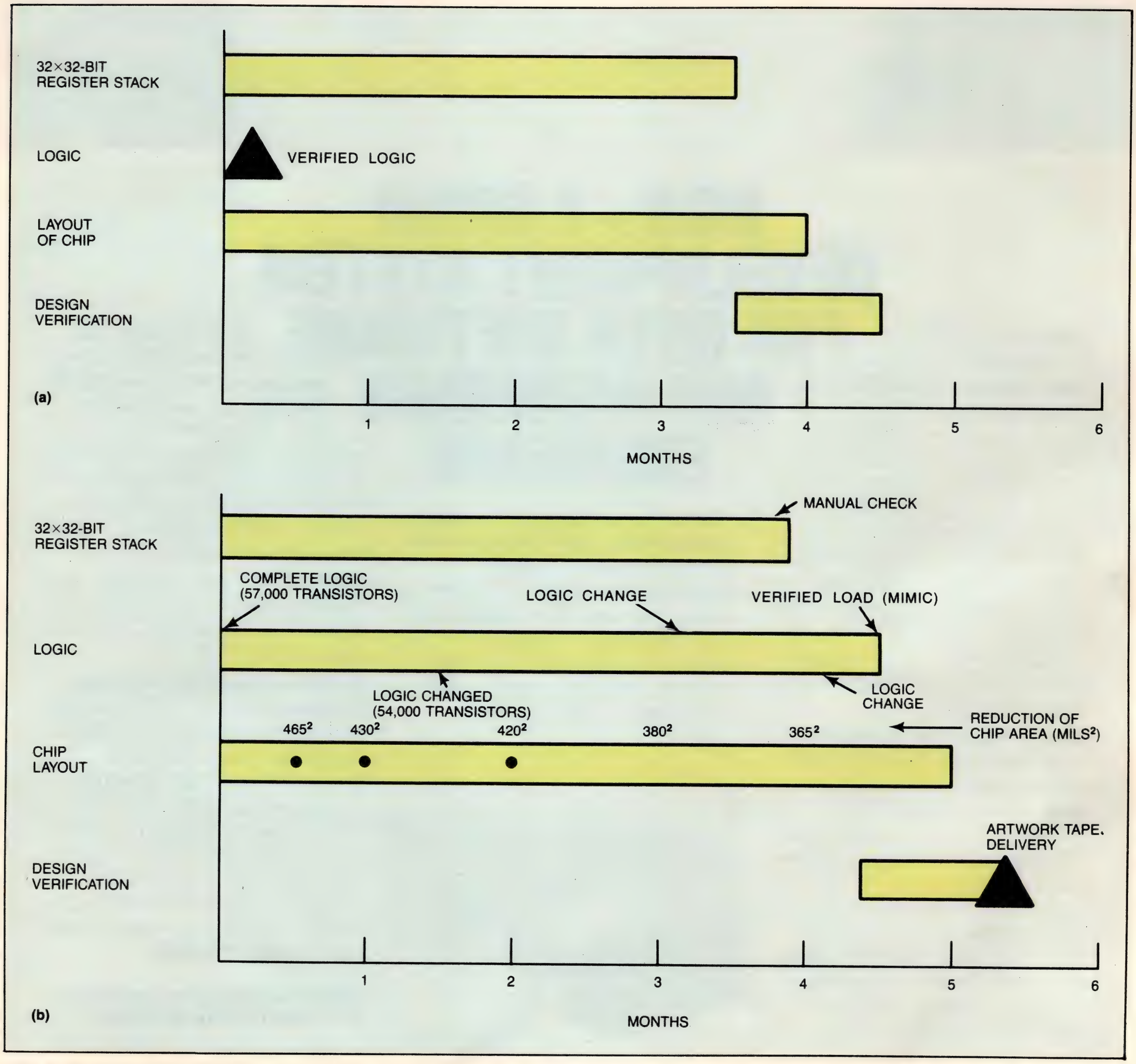


***Fig 4—Supposedly the logic was complete,*** *and thus the design and layout schedule for a 54,000-transistor μP chip **(a)** was based on the design, layout, and verification requirements for the 32×32-bit register stack. In accordance with the actual cycle **(b)**, logic design became the limiting factor for the design and layout of the chip.*

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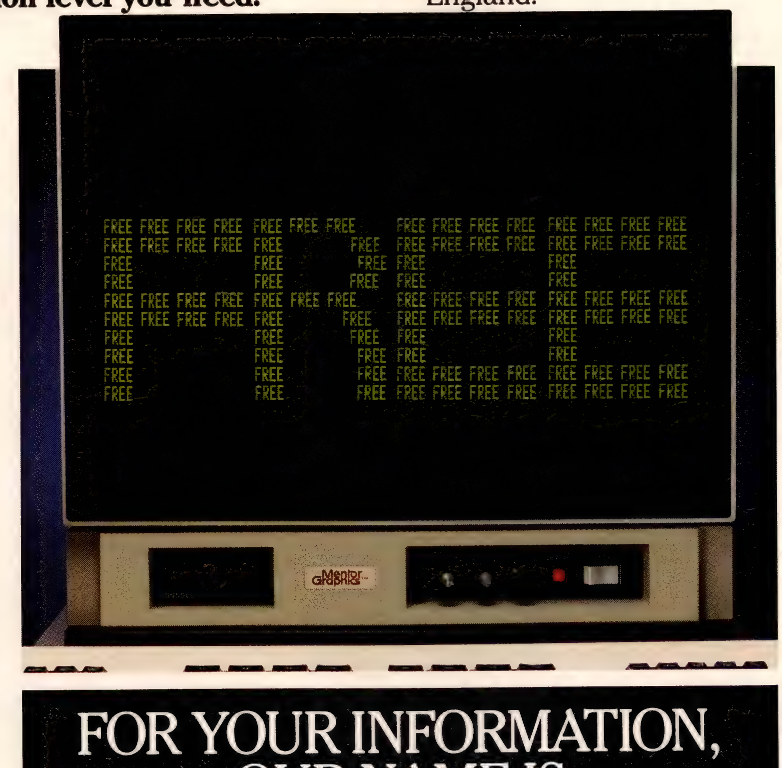

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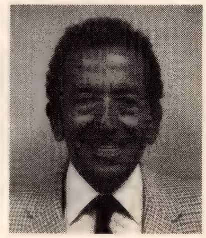
*The only effective way to determine if you have an acceptable floor plan is to implement the interconnections.*

layout of the chip. Note that a chip layout (measuring 465×465 mils) was available after the third week of the program. This layout used a macrocell outline based on preliminary estimates and reflected the state of the logic design at the time. Within these constraints, the layout was complete, and it was possible to initiate optimization techniques.

Using various design tools, the designer reduced the layout area while proceeding with the logic and macrocell designs. By the time the Mimic logic-simulator program had completed and verified the logic, chip size was 365×365 mils—about a 30% decrease from the original layout. In addition, the system also completed timing, delay, and critical-path analysis and optimization during this design period. Within a month after the logic design was completed and confirmed, the system finished the chip design, layout, and verification, and it generated an artwork tape for use in fabricating the masks. **EDN**

## Author's biography



*Albert Feller is manager of the CAD and VLSI design and development laboratory at RCA's Aerospace and Defense Div (Moorestown, NJ). Employed by the company for 34 years, he is responsible for the development and implementation of CAD tools and VSLI design techniques and aids. Al has BSEE and MSEE degrees from the University of Pennsylvania and holds three patents. In his spare time, he is an avid tennis player.*

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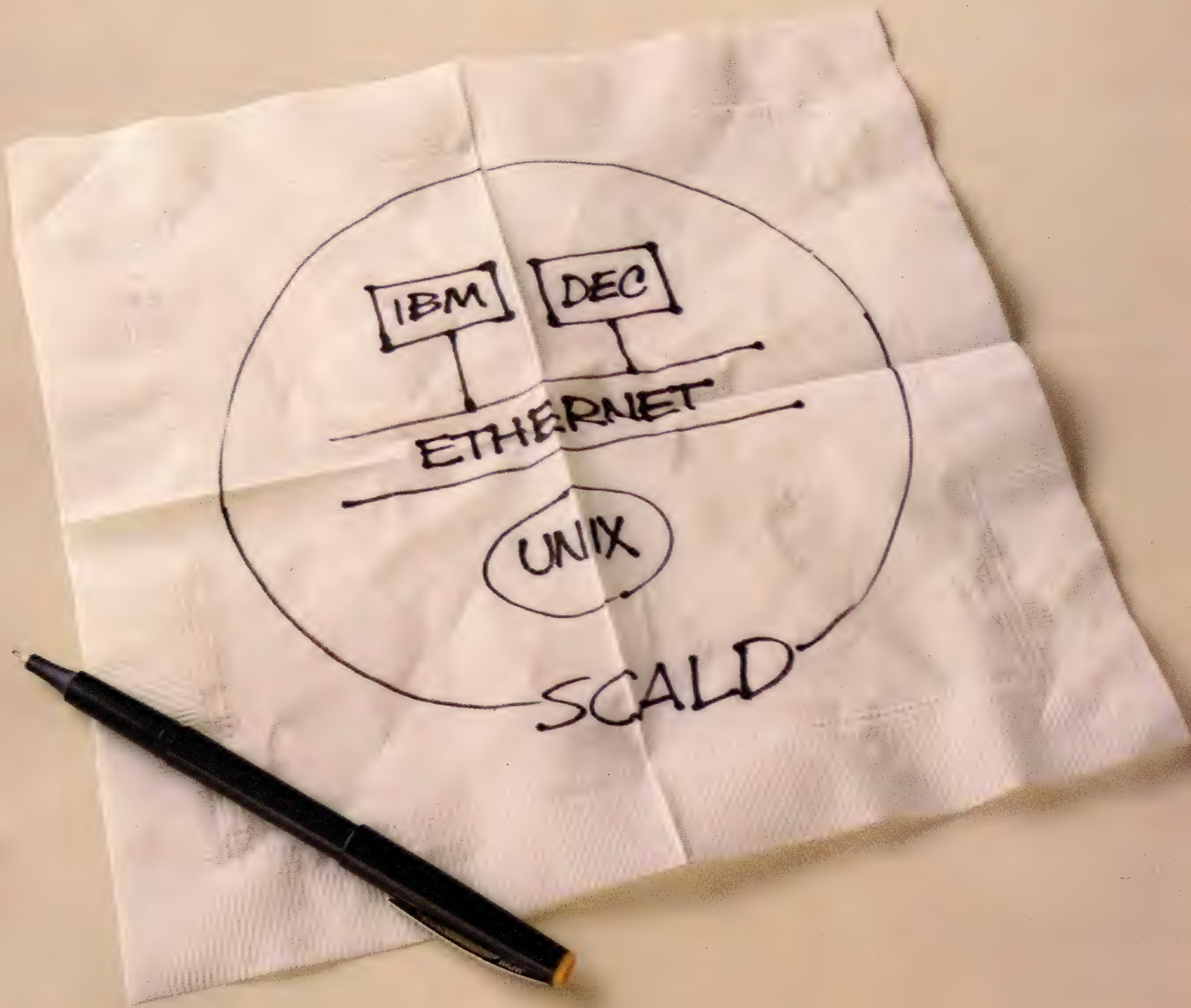


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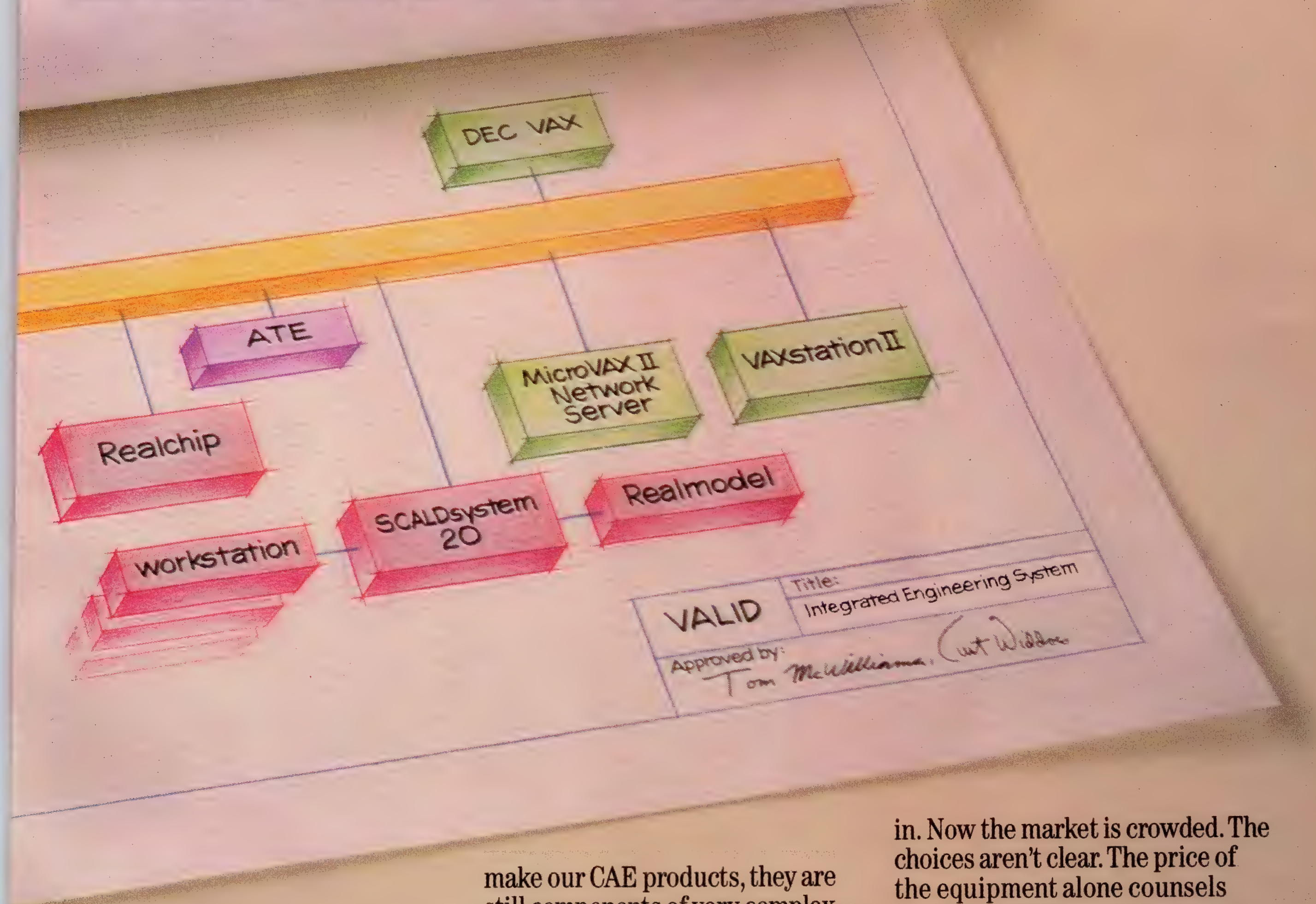


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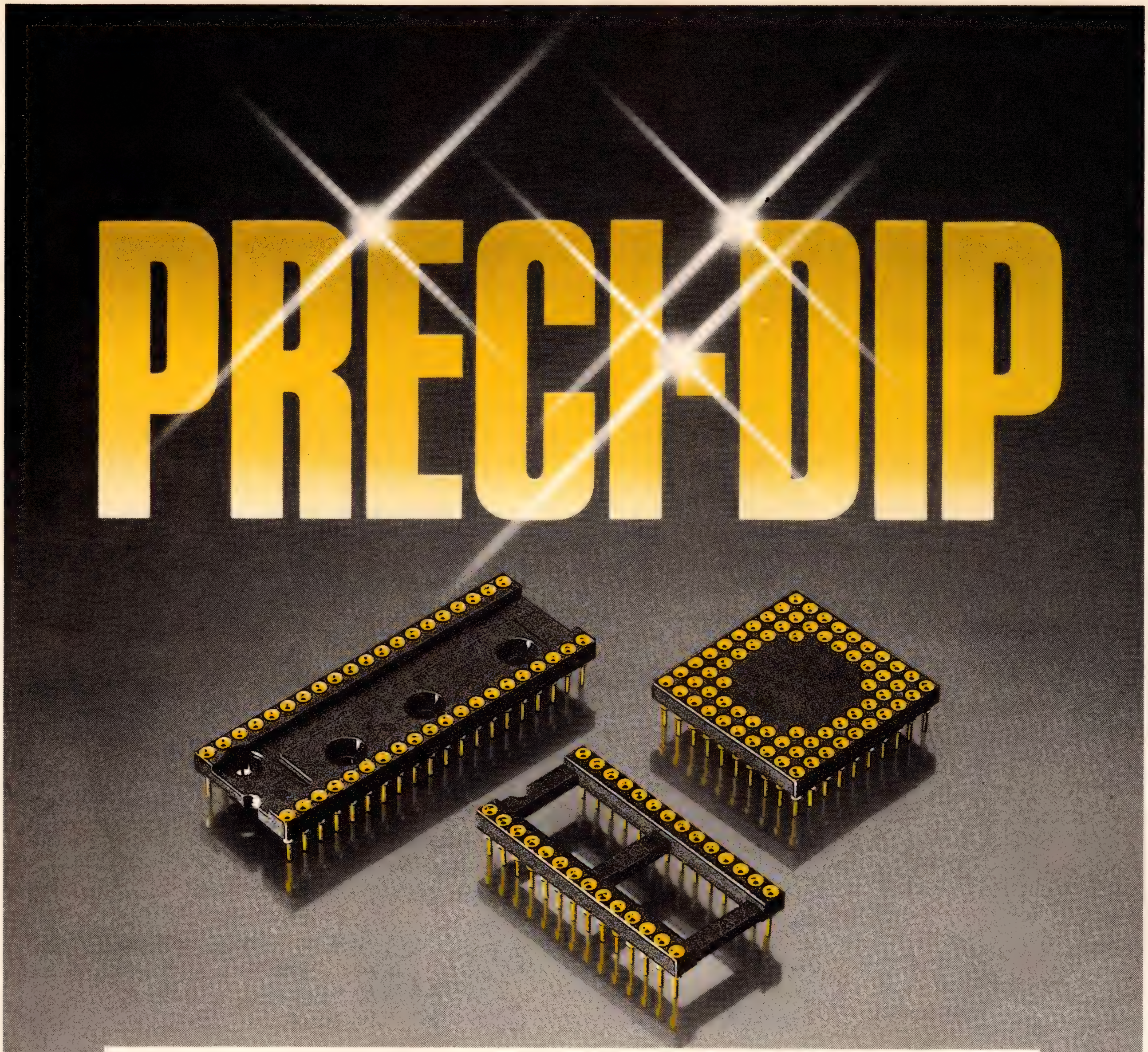


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*Balancing expandability and cost when choosing PROM/PLD programmers can be a complex task. One option is to choose a universal programmer that, when configured to program a single device family, costs no more than a dedicated programmer. With this type of universal programmer, you can add capabilities gradually.*

Alan E Negrin, *Elan Digital Systems*

Deciding which device programmer to buy isn't always simple. A dedicated programmer is capable of programming one device family. In the interests of cost and simplicity, such a programmer isn't designed to program additional device families (although it may have expansion capabilities that allow it to program newly released devices within the same family). Dedicated programmers are currently available for EPROMs and PLDs, but none are available for PROMs alone. A universal programmer, on the other hand, is capable of programming all types of semiconductor devices—plus, it might be hoped, devices that will subsequently become available.

The most economical short-term course is to purchase a dedicated programmer that meets your immediate needs. And, if you're certain that your long-term commitments will only require that you program a single device family, a dedicated programmer should suffice. But, this course might involve substantial future expense if you need to acquire additional types of programmers for other device families later.

If your short-term device-programming needs already include all families of devices, then you should have a universal programmer. It's more often the case, however, that your short-term needs require programming for only a single device family, but that your future requirements aren't clear. Thus, your selection process is more complex.

Universal programmers better serve those whose future needs aren't clearly defined. Unfortunately, many universal programmers are monolithic in their architecture, and you must pay a high starting cost for them. Nonetheless, some universal programmers are modular: You can purchase a single control unit, use it in combination with family or socket-adapter modules, and then add new modules as your programming needs expand.

Three general types of universal-programmer archi-

*A universal programmer can fill your immediate needs and allow you to be prepare for the future.*

tecture are currently in use (**Fig 1**). The first type embeds μP, display, and device-file storage directly in the programmer itself. The second type uses an embedded μP, but it relies on an attached general-purpose terminal for control and display. The third type of programmer consists of device-programmer hardware only; a general-purpose computer performs all the control, display, and storage functions. **Fig 2** depicts three universal programmers that are examples of the three respective architectures.

A universal programmer must deal with a wide number of devices and types, and these devices will continue to evolve. The variability inherent in a programmer's tasks dictates a software-controlled, μP architecture.

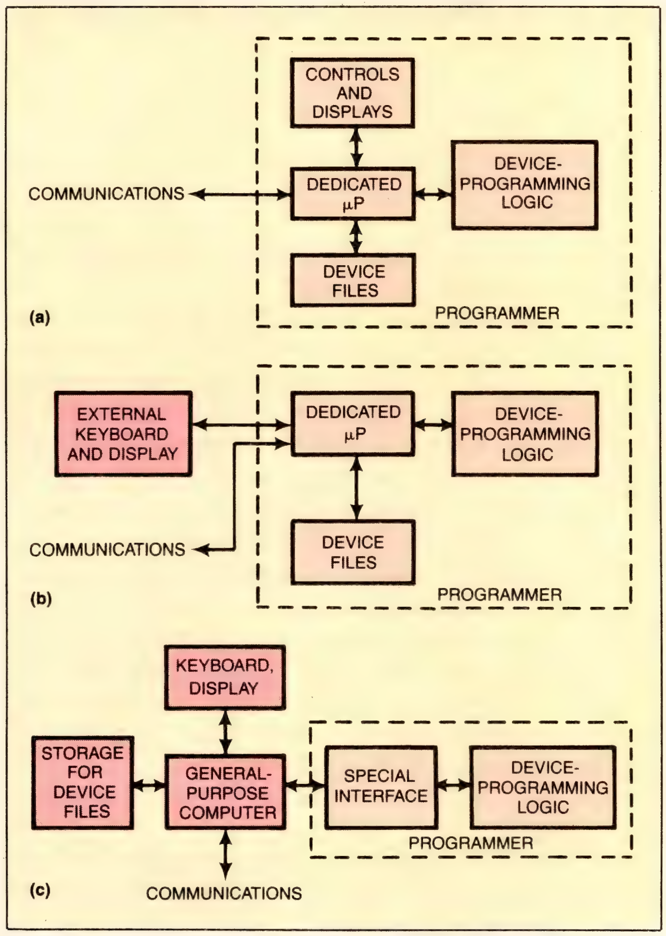



***Fig 1—Currently, you can choose between universal programmers*** *having three basic architectures: self-contained, stand-alone programmers* ***(a)****, programmers that require an external terminal for operation* ***(b)****, and programmers that employ a computer for all functions except the application programming voltages to the device to be programmed* ***(c)****.*

A programmer carries out tasks that operate in time scales of microseconds to milliseconds, and therefore real-time processor control is necessary; no remote-batch or time-sharing architecture is possible. The routines a programmer executes do not demand many instructions per second from the μP, though, so almost any modern 8- or 16-bit μP is adequate.

If you consider who will be using the programmer and the wide number of devices to be programmed, you might think that a general-purpose computer system with CRT, operating system, file management, and peripherals is the ideal processor (a personal computer, for example). But when device-programming tasks begin to require nearly full-time use of the computer system, the general-purpose label vanishes—the computer is now dedicated to device programming. When evaluating the cost of such a programmer, you must add the cost of the computer system to that of the programmer. (A similar situation can occur—to a lesser degree—with an architecture that requires an attached terminal.)

In cases that demand nearly full-time processor use, the best programmer architecture is one with processor, device storage, and display in a single unit. If the programmer has a small, low-cost CRT, its display will be cramped and hard to read. An alphanumeric display with larger, easier-to-read characters is more effective.

**Memory requirements vary**

The type and size of devices you need to program will dictate your programmer's memory requirements. Storing data for the programming of large EPROMs or vectors for verifying complex PLDs calls for the largest amounts of user programmer memory. User memory is the part of the programmer's RAM that's under control of the user and available for data storage or device testing. User memory does not include static memory or firmware used for storing device-programming libraries.

When programming EPROMs, enough user memory must be available for data storage for all EPROMs being programmed simultaneously. If you needed to program as many as eight different 512k-bit EPROMs at one time, for example, you'd need 4M bits (512k bytes) of user memory. This 4M bits is probably the maximum requirement for the foreseeable future.

Verification of complex PLDs requires storage of vectors, which have a bit for every input and output variable. A complete test for a large PLD might require

several thousand different vectors. Because the most complex PLDs expected in the near future will probably use no more than 64 input and 64 output variables, you may need several hundred thousand bits of storage for such vectors. This amount, however, is still less than that required for large EPROMs.

If a programmer uses a computer as its controller, only the user memory that's really free can be counted as available for device programming. You must subtract the operating system and the programmer's software, plus other resident tasks from the total user RAM of the computer to calculate the user memory that's actually available.

### Communications is requisite

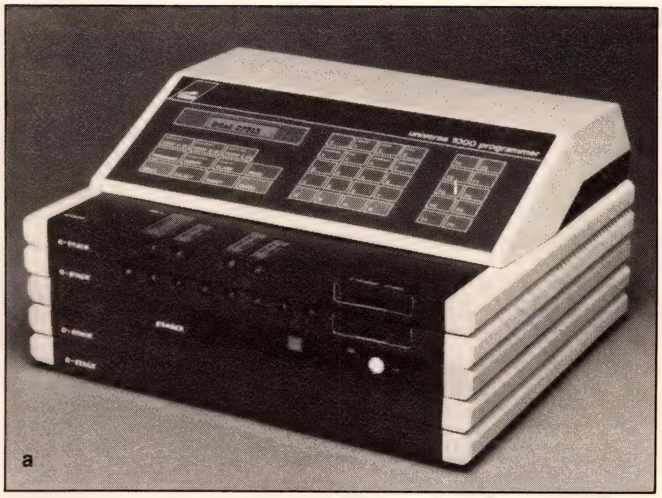
Whatever the structure of a universal programmer's processor and memory, a programmer must be able to communicate with other computers or development systems because the programmable device's data is almost always in computer-generated files. Depending on the type of device to be programmed, this data-file source can be a mainframe computer, a personal computer, or a μP development system.

Most communications required between a programmer and its various hosts use RS-232C serial links with various formats and speeds. In order to deal with these variations, you should be able to simply select, from a menu, the appropriate data format and speed. A well-equipped menu should offer selections of 10 to 15 of the most common formats and should allow speeds from 50 to 19,200 baud. Almost no host computer can transmit faster than 19,200 baud on a serial port.

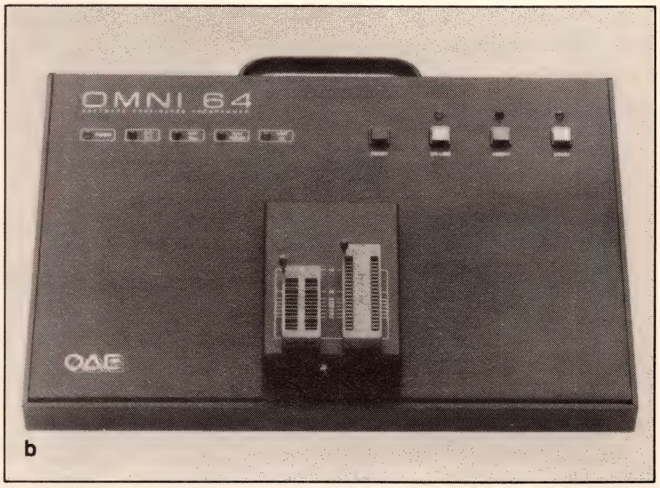
If your universal programmer is intended as a resource for a large development laboratory, you may find a networking interface (Ethernet or some similar system) essential to allow all users access. Thus, it's desirable for a programmer's architecture to have an additional I/O port available for a networking interface. You can also use such a port for an interface to a label printer or device handler.

Using a universal programmer as a resource in a development lab often requires that a host computer control the programmer rather than that the programmer have its own manual controls. Thus, in addition to a serial communications interface, the programmer must possess a remote-control capability: The host computer must be able to control the programmer via commands transmitted over the communications channel.

Because semiconductor manufacturers are continually introducing new families of programmable devices




a

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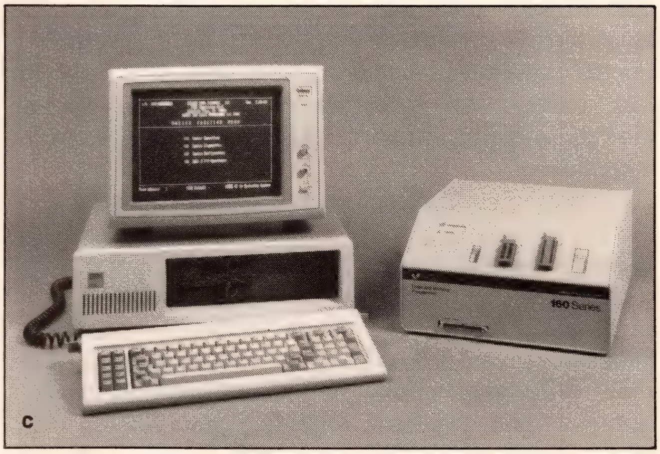


c

***Fig 2—Three universal programmers****—the Elan Digital Systems Universe 1000* ***(a)****, the Oliver Advanced Engineering Omni 64* ***(b)****, and the Valley Data Sciences Model 160* ***(c)****—offer, respectively, the architectures depicted in* ***Fig 1a, 1b,*** *and* ***1c.***

*Three general types of universal-programmer architecture are currently in use.*

## UNIVERSAL-PROGRAMMER ARCHITECTURES

| TYPE OF ARCHITECTURE | COMMENT |
|---|---|
| EMBEDDED PROCESSOR AND DISPLAY | COST/FEATURE COMPROMISE |
| EMBEDDED PROCESSOR, EXTERNAL DISPLAY REQUIRED | FLEXIBLE, MORE COSTLY |
| ATTACHED PERSONAL COMPUTER REQUIRED | FLEXIBLE, COSTLY FOR APPLICATIONS IN WHICH PROGRAMMER (AND HENCE COMPUTER) SEES FULL-TIME USE |
| NO PROCESSOR | INFLEXIBLE, NO COST ADVANTAGE |
| **USER MEMORY** | |
| 512k BYTES OR MORE | ADEQUATE FOR TODAY'S MAXIMUM EPROM-DATA AND PLD-TEST-VECTOR STORAGE REQUIREMENTS |
| 64k TO 511k BYTES | ADEQUATE FOR TODAY'S MAXIMUM TEST-VECTOR STORAGE NEEDS |
| LESS THAN 64k BYTES | MEETS FEW MAXIMUM NEEDS |
| **FIELD-UPGRADE METHODS** | |
| CARTRIDGE | CONVENIENT TO USE, EASY TO CHANGE, AND LOW COST |
| FLOPPY DISK | CONVENIENT TO USE AND EASY TO CHANGE, BUT PROGRAMMER COST IS HIGHER |
| INTERNAL PART CHANGE | CLUMSY TO USE AND DIFFICULT TO CHANGE, BUT PROGRAMMER COST IS LOWER |
| PERSONALITY MODULE | CLUMSY TO USE AND CHANGE, ADDITIONAL MODULES ARE EXPENSIVE |
| **FAMILY-CHANGE METHODS** | |
| PERMANENTLY INSERTED PLUG-INS THAT CONTROL PROGRAMMING VOLTAGES AND TIMING | EXPANDABLE, FLEXIBLE, AND EASY TO USE |
| EXCHANGEABLE PLUG-INS THAT CONTROL PROGRAMMING VOLTAGES AND TIMING | EXPANDABLE AND FLEXIBLE, BUT CLUMSY TO USE |
| PLUG-INS THAT DON'T CONTROL PROGRAMMING VOLTAGES AND TIMING | EXPANDABILITY MIGHT BE LIMITED |
| FIXED SOCKETS, NO ADAPTERS | INFLEXIBLE AND NOT EXPANDABLE |

and new devices within existing families, programmers eventually require firmware upgrading in the field in order to allow users who have already bought programmers to take advantage of the latest programmable devices. The earliest strategy for field upgradability was the personality module. This module was a plug-in card, which could replace another card with different interface circuitry when a different device was to be programmed.

As devices multiplied, however, the number of personality modules required became great, and their cost became excessive. Such a great number of personality modules became difficult to store and track and were apt to wear out if inserted and extracted too many times. Moreover, it was often difficult to correlate the device to be programmed with the proper personality module without elaborate reference charts.

As technology evolved, new programmers were designed without personality modules. These new programmers allowed you to select the device to be programmed from a menu (which listed only the devices available at the time of the programmer's manufacture). The programmer then applied the proper sequence of voltages from its variable internal power supplies to the device being programmed.

Manufacturers of programmers employing menu-driven device selection needed a way to modify their programmers firmware in the field as new devices became available. Manufacturers often asked users to return programmers to the factory, where device programming firmware (stored in EPROMs) was upgraded. In some cases, manufacturers would merely send out EPROMs containing new firmware and ask their users to disassemble their programmers and replace the EPROMs themselves.

Technically unsophisticated users, however, sometimes made mistakes in exchanging EPROMs, causing programmer malfunctions, which sometimes turned out to be hard to track down. The other option, returning the programmer to the factory for updates, although generally foolproof, represented weeks of lost productivity.

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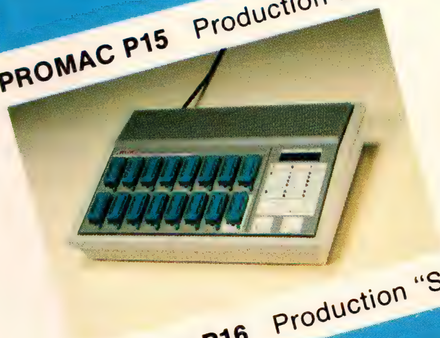

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*A complete test for a large PLD can require several thousand different vectors.*

A better solution turned out to be some sort of removable media, such as cassettes, cartridges, or floppy disks, that could store software updates. Thus, programmer manufacturers could simply send firmware for new devices to all users, allowing users to update their own equipment without risk of programmer malfunction, and without losing the use of the programmer during the manufacturer's updating process.

Programmers designed for use in conjunction with personal computers generally use floppy disks. Some stand-alone programmers use EPROM cartridges, like those used in video games, which provide the same level of convenience as floppy disks and are also low in cost. Other stand-alone programmers use floppy disks, but the additional interfaces and controllers required to support these disks makes the hardware for a system using them more costly than one using EPROM cartridges.

**Family adapters are desirable**

In addition to accommodating firmware upgrades, programmers also require hardware upgrading when new families are introduced. Family modules that plug into a master control unit can solve the problem of hardware upgrading. If device manufacturers announce a new family of semiconductors, and the existing family plug-ins can't provide support, then the programmer manufacturers can release a new family plug-in.

"Permanently inserted" family modules (ones that can handle an entire family of devices) are more convenient to use than ones that you must frequently plug in and extract. The latter type of family plug-ins start to manifest the same difficulties as the personality modules; the plug-ins get lost, pins get damaged, and users have difficulty correlating devices with the proper plug-ins.

The family plug-ins should generate all pin connections and all programming voltages and currents internally. This strategy preserves the expandability of the programmer's master control unit. If the control unit of the programmer provides the programming voltages, new device families with more pins than anticipated, or with different voltage requirements, may not be programmable without major internal changes to the programmer's control section.

At this time, at least four different EPROM pinouts, seven different PROM pinouts, and (depending on which devices you count as actually being available), eight or nine different PLD pinouts exist. Semiconductor manufacturers currently contemplate additional pin configurations for newer devices as well. Further, they have announced newer packages for existing devices: Miniature DIPs, LCCs, pin-grid arrays, and surface-mount types are all in the works at various semiconductor development laboratories.

If a programmer is to be prepared to accommodate new pinouts and device packages, it needs some sort of socket-adapter strategy in addition to family adapters. Optimally, socket adapters should be available for every family adapter because new packaging can come along for even widely available devices. Because you may need many such adapters, you should choose a programmer that utilizes inexpensive adapters consisting of passive components only. **EDN**

## Author's biography

*Alan E Negrin is president of Elan Digital Systems in Palo Alto, CA. He previously worked as the vice president of Harris Digital Telephone Systems and as a manager at Rank Xerox Data Systems. Al obtained a BSEE from the University of California at Berkeley and an MSEE from Stanford. In his spare time he enjoys tennis, jogging, and reading science fiction.*

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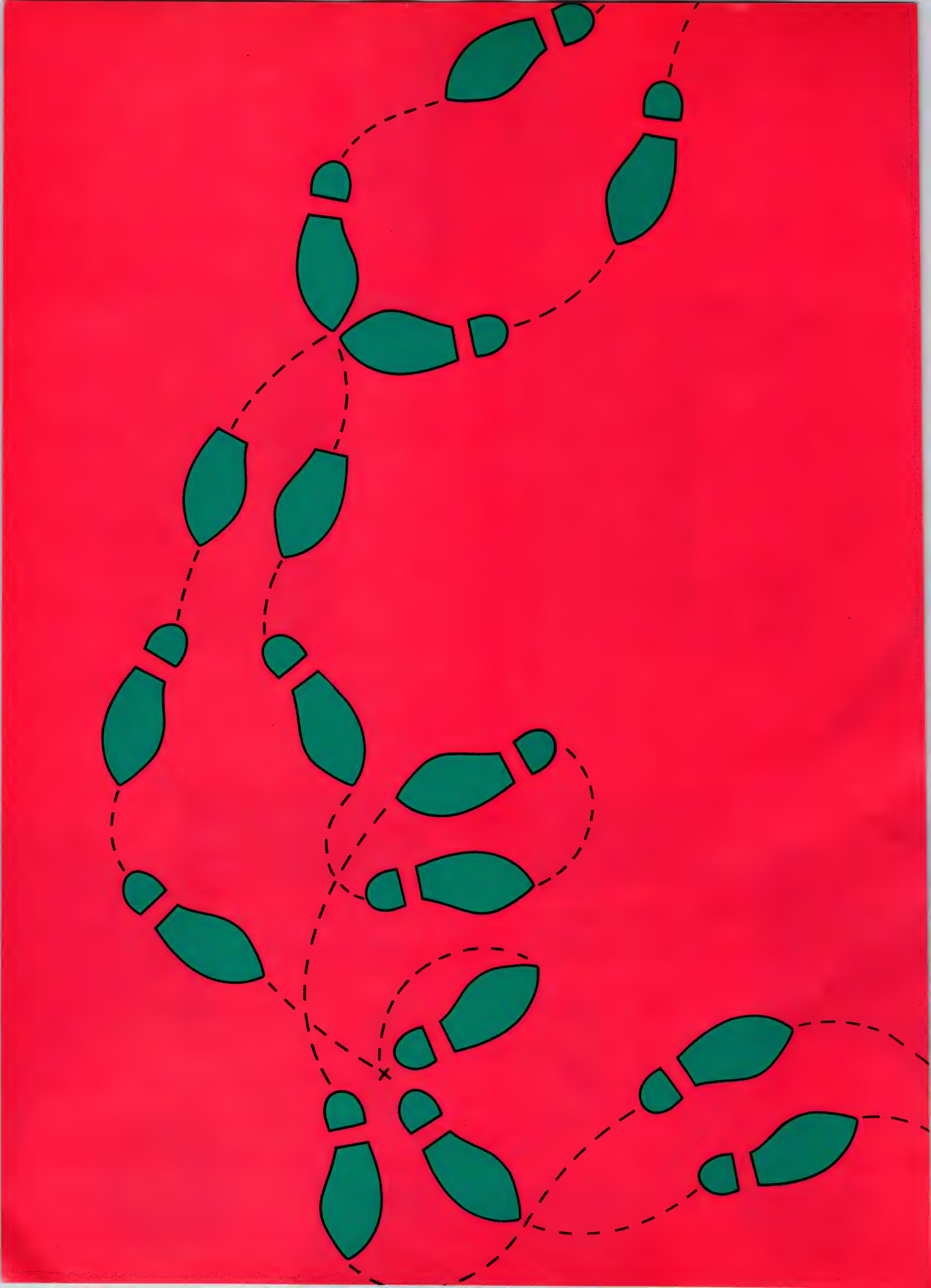

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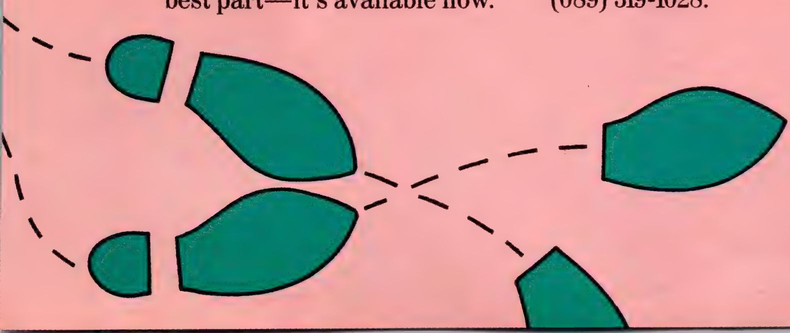

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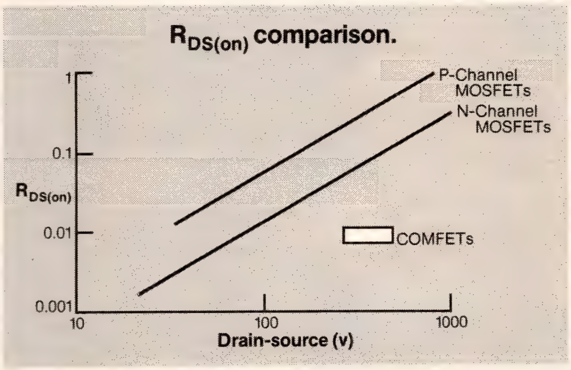


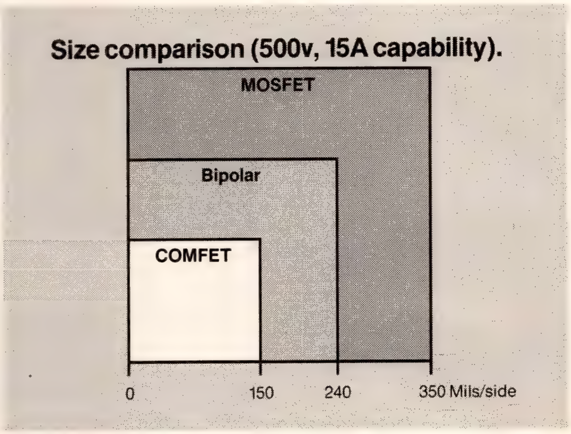


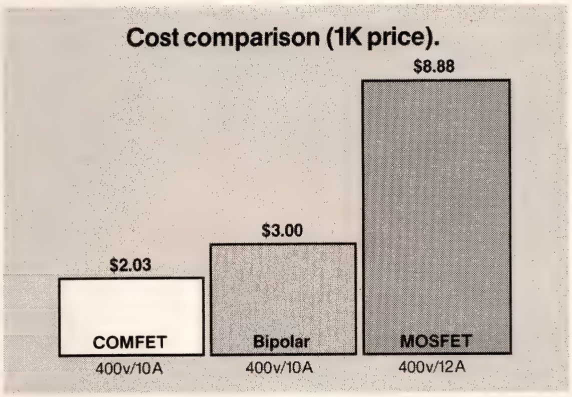


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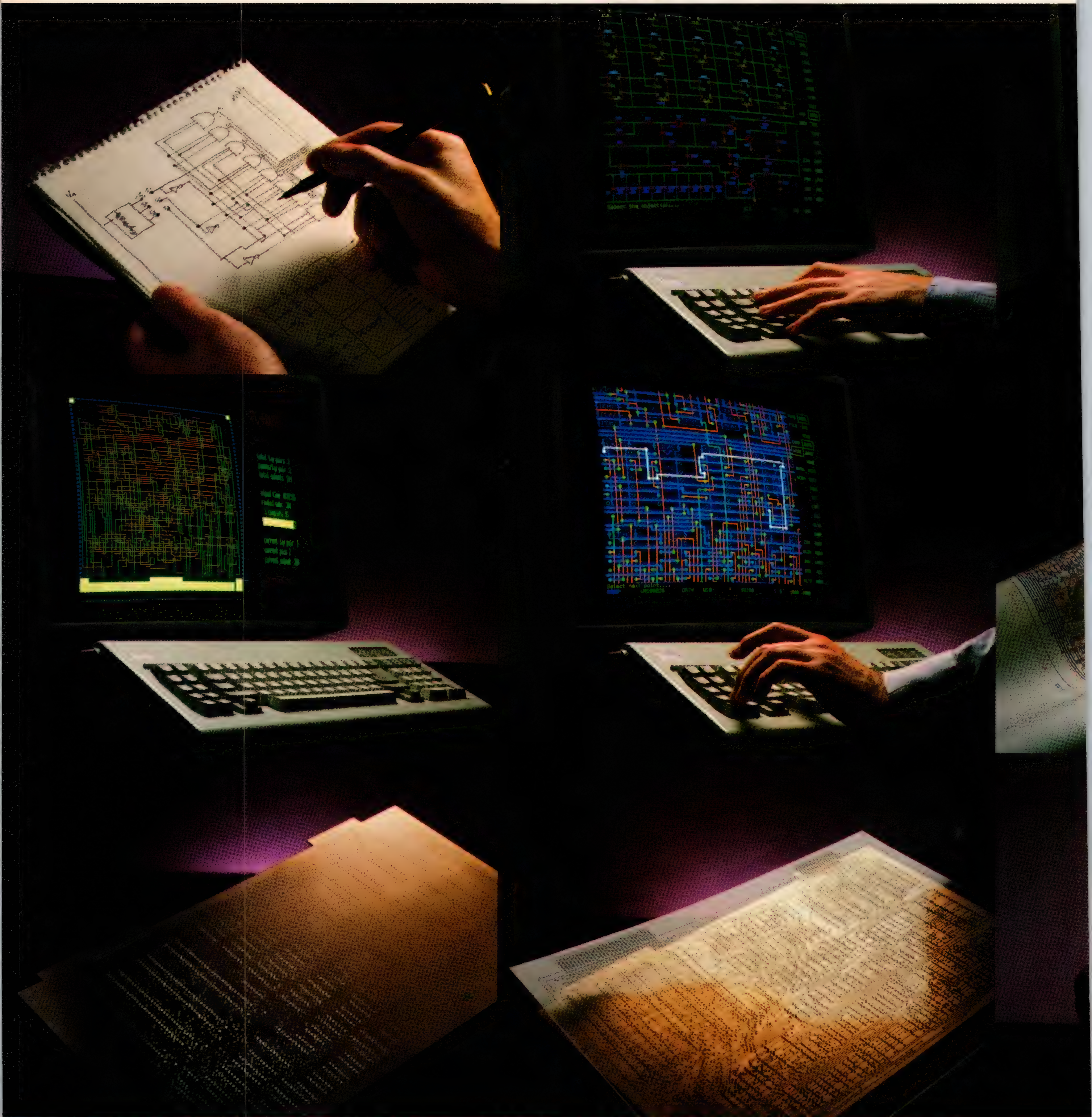

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# Op amp improves V/F converter's input

Jerry Graeme
*Burr-Brown Corp, Tucson, AZ*

By adding an op amp to a V/F converter, you can combine the highly linear A/D-conversion capability of the converter and the high-impedance differential input of an instrumentation amplifier (IA). This approach eliminates the separate IA that's often required for preamplification and rejection of common-mode noise.

You connect the op amp to the input integrator of a charge-balance type of V/F converter **(Fig 1a).** This combination leaves two high-impedance inputs, which impress their difference signal across the integrator's input resistor $R_1$. You choose that resistor value to set the V/F converter's gain as though it were an IA. (For the VFC320 V/F converter shown, set the resistor value to produce 0.25 mA for a full-scale differential input.) Then, choose the desired output pulse width ($C_1$ value) and the integrator output swing ($C_2$ value). For the component values shown, a 1V differential input will produce a 10-kHz full-scale output. The relation is

$$F_O=(E_2-E_1/(7.5R_1C_1).$$

A common-mode voltage will create no signal current in $R_1$, but it will shift the integrator's output, causing a change in trip-time for the following comparator. One V/F-converter cycle removes most of this timing error, however, because the integrator capacitor absorbs the common-mode voltage, and feedback via the reset current source restores the integrator's output. Moreover, during gain calibration the linear portion of the common-mode error disappears; only the nonlinear portion (approximately 10%) contributes to the overall nonlinearity. For this circuit, gain nonlinearity is 0.03% typ.

AC common-mode signals affect the timing of every V/F-converter cycle, but the net effect is 0, provided that the count period (for reading the V/F converter) is long compared to the period of the common-mode signal.

Because this technique increases the integrator's gain, it also increases the output offset and the gain nonlinearity. Gain nonlinearity, for example, increases according to (approximately) the V/F converter's normal 10V full-scale input range divided by the new full-scale value. Further, you are limited by the V/F converter's common-mode rejection capability (60 dB) and common-mode range (−10 to 1V). To increase the common-mode range (to −5 to 10V), connect the op amp output to the V/F converter's common return (**Fig 1b**). This connection also shifts the output pulses' zero level, so you may have to add the level-translating transistor $Q_1$. **EDN**

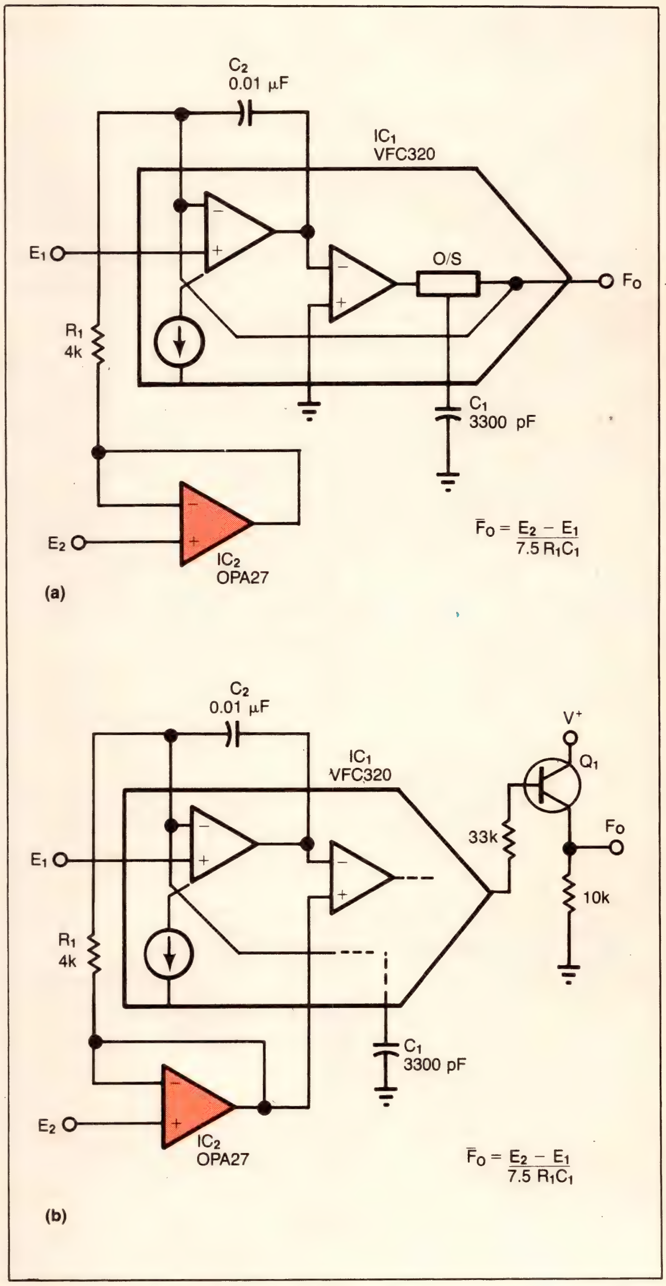


***Fig 1—Adding an op amp ($IC_2$)** provides a V/F converter ($IC_1$) with preamplification and high-impedance differential inputs **(a)**. The connection in **b** extends the common-mode voltage range from −10 to 1V to −5 to 10V.*

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# Dual op amp forms RS-232C driver/receiver

Jean-Paul Lambrechts
*National Semiconductor, Santa Clara, CA*

To provide a single interface between an RS-232C line and a MOS LSI chip while saving board space and power, you can use a dual op amp **(Fig 1)** in place of the traditional 1488-type line driver and 1489-type line receiver. Further, the LF353N op amp handles transmission rates as high as 19,000 baud without exceeding the EIA's specification for maximum slew rate.

When node B is high, clamping action of the zener diode $D_2$ keeps op amp $IC_{1A}$ in its linear region of operation. The 3.3V zener voltage is impressed across resistor $R_3$, which injects a constant current (84 μA) into node A. The resulting voltage at node A, by a Thevenin-equivalent analysis, is 1.82V; thus, node B is 1.82+3.3=5.12V (7V is the maximum allowed by $IC_2$). This 5.12V output at $IC_{1A}$ is stable for all bipolar-low levels normally encountered at the RS-232C line input, ie, −2V and below for most terminals.

As the line input rises to the high level, the node A voltage decreases, causing the current through $D_2$ to reverse direction for some input level below 1.82V. The resulting forward bias across $D_2$ (0.7V) causes node A to drop to 0.85V, yielding 0.85−0.7=0.15V at node B. The circuit is actually a Schmitt trigger that behaves as a voltage regulator in both stable states. That is, node B assumes 0.15V for inputs above 0.91V and assumes 5.12V for inputs below approximately 0V.

In the line-driver section, op amp $IC_{1B}$ acts as a comparator, with the node A voltage (0.85 or 1.83V) on its noninverting input. The corresponding serial output (SO) of $IC_2$ is 2.4 or 0.4V, so $IC_{1B}$ inverts the SO signal as desired. Diodes $D_1$, $D_3$, and $D_4$ provide overvoltage protection, and $R_6$ limits the current exchanged with the line. EDN

**To Vote For This Design, Circle No 750**

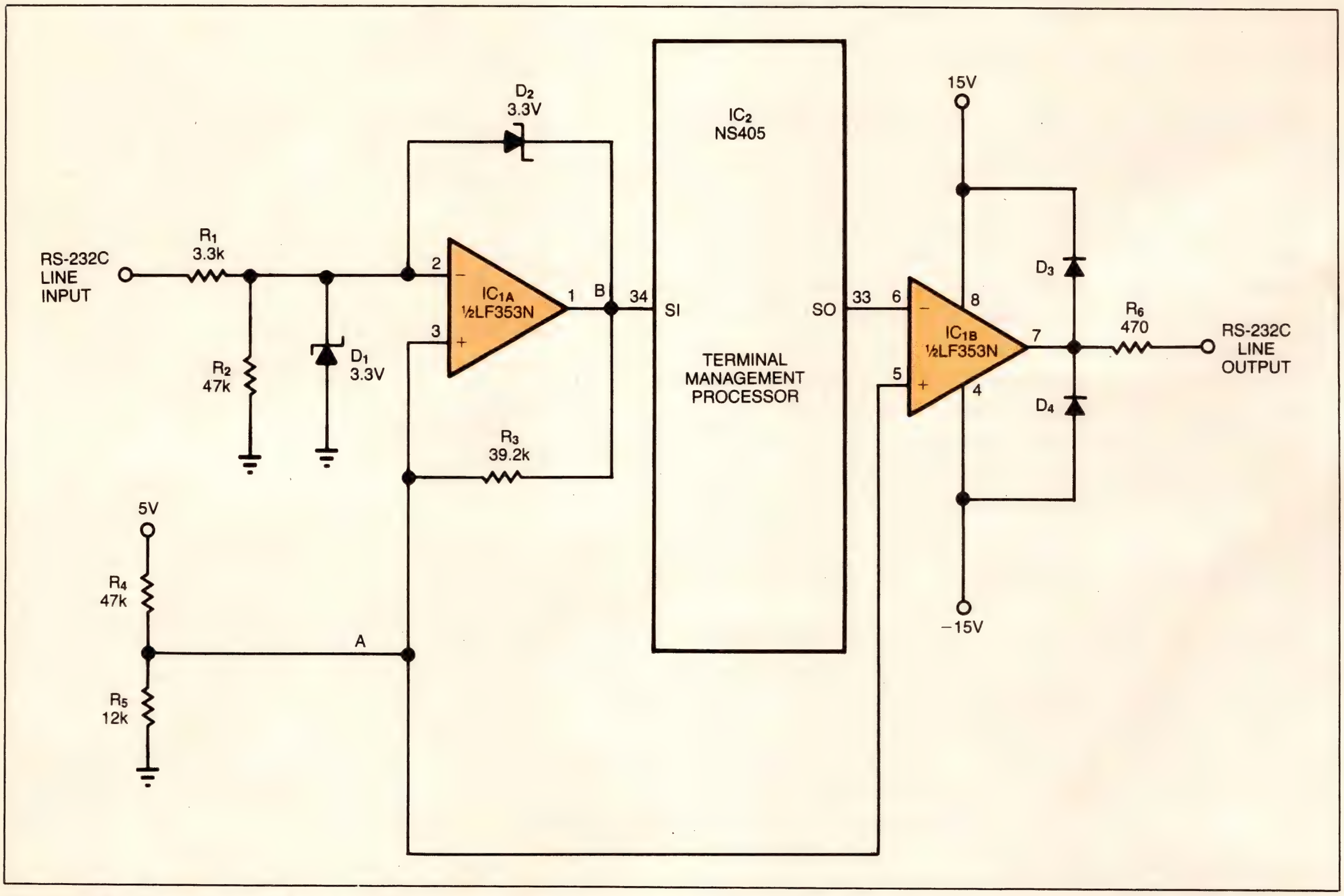


*Fig 1—A dual op amp provides a single-channel interface between an RS-232C line and a MOS terminal-management IC.*


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|---|---|---|---|---|---|---|---|---|---|---|---|---|
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| Max. 20dB Stop Frequency (MHz) | 19 | 70 | 147 | 210 | 290 | 410 | 580 | 750 | 840 | 1000 | 1100 | 1340 |

Prices (ea.): P $9.95 (6-49), B $24.95 (1-49), N $27.95 (1-49), S $26.95 (1-49)

| HIGH PASS Model *HP– | 50 | 100 | 150 | 200 | 300 | 400 | 500 | 600 | 700 | 800 | 900 | 1000 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
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*Prefix P for pins, B for BNC, N for Type N, S for SMA    *example:* **PLP-10.7**

**CIRCLE NO 145**

C105 REV. ORIG.

# Algorithm generates a list of combinations

Charles P Capps
*General Motors Corp, Goleta, CA*

Using the method described here, you can generate a list of all possible combinations for a large number of items, either by hand or with the aid of a computer. You can easily produce a list for four or five items with or without this method; however, generating a list of six or more entities without this procedure would be a formidable task.

First, form an array vector A in which $n$ corresponds to the total number of elements, eg, A(1), A(2), . . . A(n). Next, generate a 2-dimensional array B(J,K) in which J ranges from 1 to $(2^n-1)$ and K ranges from 1 to n. Fill each row with the binary number for that value of J. Then, multiply each element of A by the corresponding element in the first row vector of B, and repeat—multiplying each row vector of B by the vector A. Thus, in each row, the elements of A are multiplied by a 1 or a 0. Dropping those elements multiplied by 0, you are left with a table of possible combinations.

As an example, consider a group of three entities, x, y, and z. The vector A becomes A(1)=x, A(2)=y, and A(3)=z, and the array B looks like **Fig 1.** Now, multiply the row elements of B by corresponding elements of A. For row six, the result is as follows:

$$B(6,1)\times A(1)=1\times x=x$$
$$B(6,2)\times A(2)=1\times y=y$$
$$B(6,3)\times A(3)=0\times z=0.$$

**ARRAY B**
(COLUMN)

| (ROW) | 1 | 2 | 3 |
|---|---|---|---|
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |

***Fig 1—This array helps you list** all possible combinations of n elements (in this example, n=3). The array has n columns and $(2^n-1)$ rows.*

Combining the results of all multiplications, you end up with three combinations for three entities used one at a time (x, y, and z); three combinations for three entities used two at a time (x,y), (y,z), and (x,z); and one combination for three entities used three at a time (x,y,z).

You need write the array B only once, and if it's contained in a program, you can store it as a data file and call it as needed. Further, you can write a program that lists only a subset of the possible combinations. By noting the sum of nonzero elements in each row, the program can list only the combinations for groups of three or less, four or more, etc. **EDN**

**To Vote For This Design, Circle No 746**

# Digital power controller handles 1 kW

John A Haase
*Colorado State University, Fort Collins, CO*

With this power controller **(Fig 1)** you can vary the power to a load according to a 2-decade BCD word, obtained either manually or from a computer. For an open-loop system you can deliver at least 1 kW to a resistive load, in 1% increments (0 to 99%). Or, you can combine the controller with a sensor and heater, for example, to regulate temperature. The controller delivers an integral number of line cycles every 1.67 sec; switching occurs near the zero-voltage crossing so the load current has no dc component.

AC line voltage is regulated to about 7V by $IC_1$ for use as a supply voltage ($V_S$). The zero-crossing detector $IC_2$ also takes its supply voltage directly from the line via $R_4$ and $R_5$. In addition, the line drives the 4N26 optocoupler, producing a 60-Hz clock signal to the rate

multipliers $IC_3$ and $IC_4$.

The cascaded rate multipliers accept a 2-decade BCD word and provide an output (pin 6, $IC_3$) of one-tenth the word value times 60 Hz. (In this system, you enter the control word manually using the quad switches $S_1$ and $S_2$.) The shunting effect of $R_5$ ensures that the LED $D_4$'s on-period is well within a positive half-cycle of the line voltage (**Fig 2**). Consequently, the count-advance

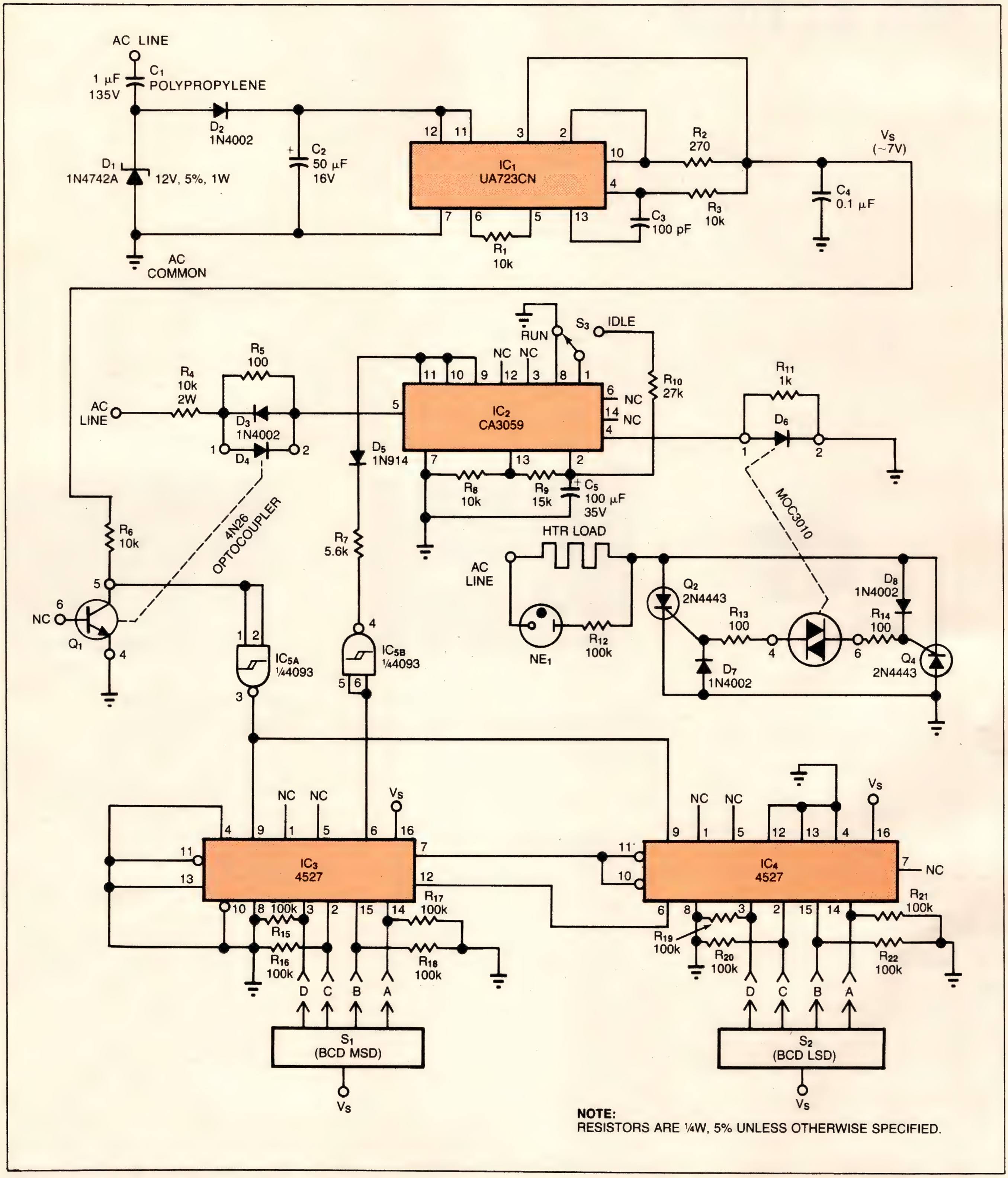


*__Fig 1—A low-power circuit provides digital control__ of 1 kW, or more, in 1% steps. A zero-crossing detector ensures that only an integral number of full line cycles reach the load during any 1.67-sec control period.*

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pulses from $IC_{5A}$ to the rate multipliers occur once per line cycle and in advance of the zero crossing.

Then, for each output pulse via the Schmitt trigger $IC_{5B}$, the zero-crossing detector $IC_2$ emits two pulses at pin 4, which are optically coupled to the gates of SCRs $Q_2$ and $Q_4$. As a result, the appropriate SCR turns on during two consecutive half-cycles of the line voltage (highlighted areas in **Fig 2**).

This circuit can replace an autotransformer in many applications, offering less weight, less volume, and better control resolution. The circuit also has the following characteristics:

- $S_3$ is an on-off switch—no power to the load in the idle position.
- Brightness of the neon lamp $NE_1$ gives an approximate indication of load power.
- Power switching is optically isolated from the control circuits.
- No partial- or half-cycles of line voltage are delivered to the load.
- Power cycles are uniformly spaced for power-of-2 control words. Note, however, that other control words may cause a noticeable variation in power over the 1.67-sec control interval.

**EDN**

**To Vote For This Design, Circle No 749**

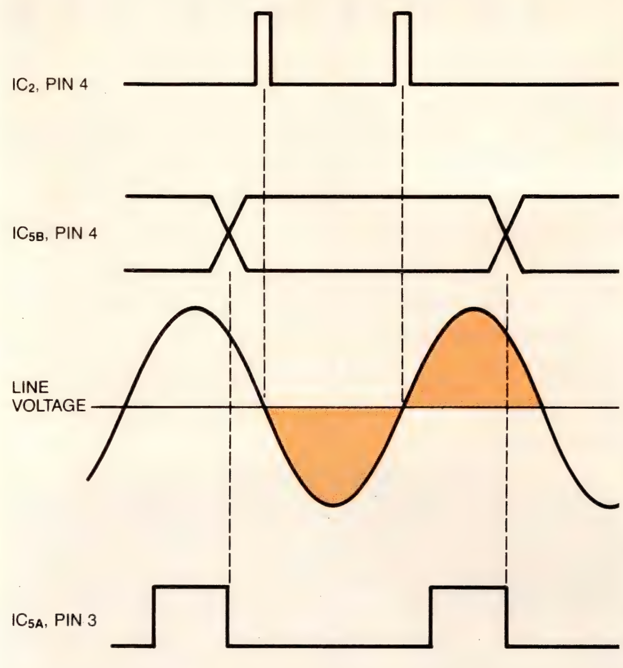


***Fig 2—This circuit is timed to fire the SCRs $Q_2$ and $Q_4$ (Fig 1)*** *so that only one full line cycle (highlighted area) is passed to the load for each pulse from $IC_{5B}$, pin 4.*

# Software provides indirect call for μC

Allen Moore
*Sundstrand Data Control, Redmond, WA*

Although the 8051 microcomputer doesn't have an indirect-call instruction, you can implement one with a few lines of code. Your routine's address can reside in any two bytes of internal data memory. In **Listing 1**, the routine's address is in the data pointer (DPTR). The routine must end with a "ret" instruction.

*(Ed Note: This technique is applicable to other processors as well. Note that, in* ***Listing 1,*** *the "ret" instruction returns the program to a routine at the address contained in dpl and dph. This routine (not shown) will require an additional "ret" instruction to vector the program counter to the instruction "sjmp done".)* **EDN**

**To Vote For This Design, Circle No 747**

**LISTING 1**

```
         lcall   caller      ;put return address on stack
         sjmp    done

                             ;put address of routine to
                               be called on stack
caller:  push    dpl         ;low byte first . . .
         push    dph         ; . . . then high byte
         ret                 ;'call' @DPTR

done:
```

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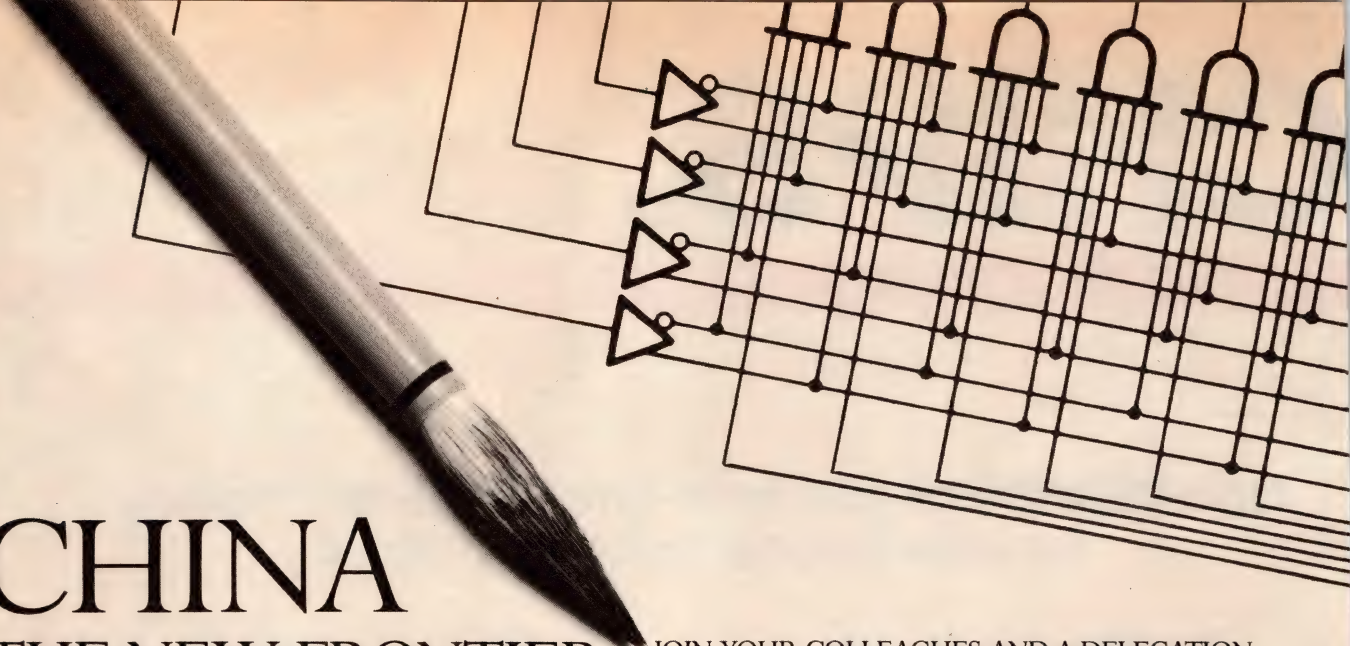

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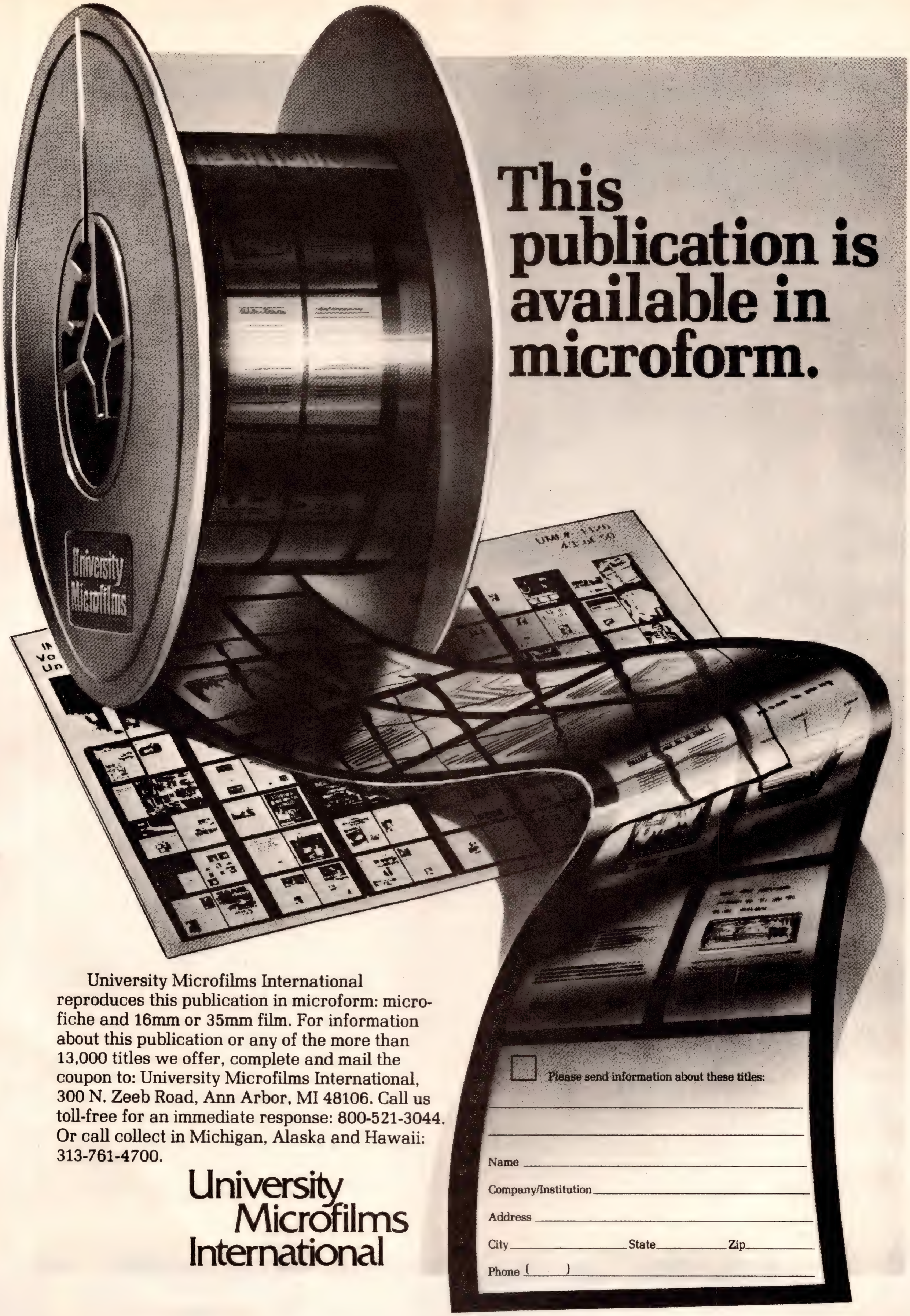


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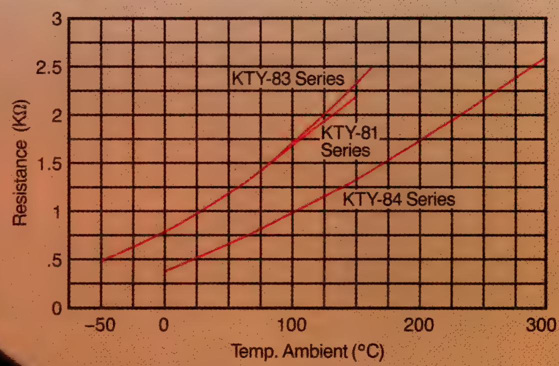


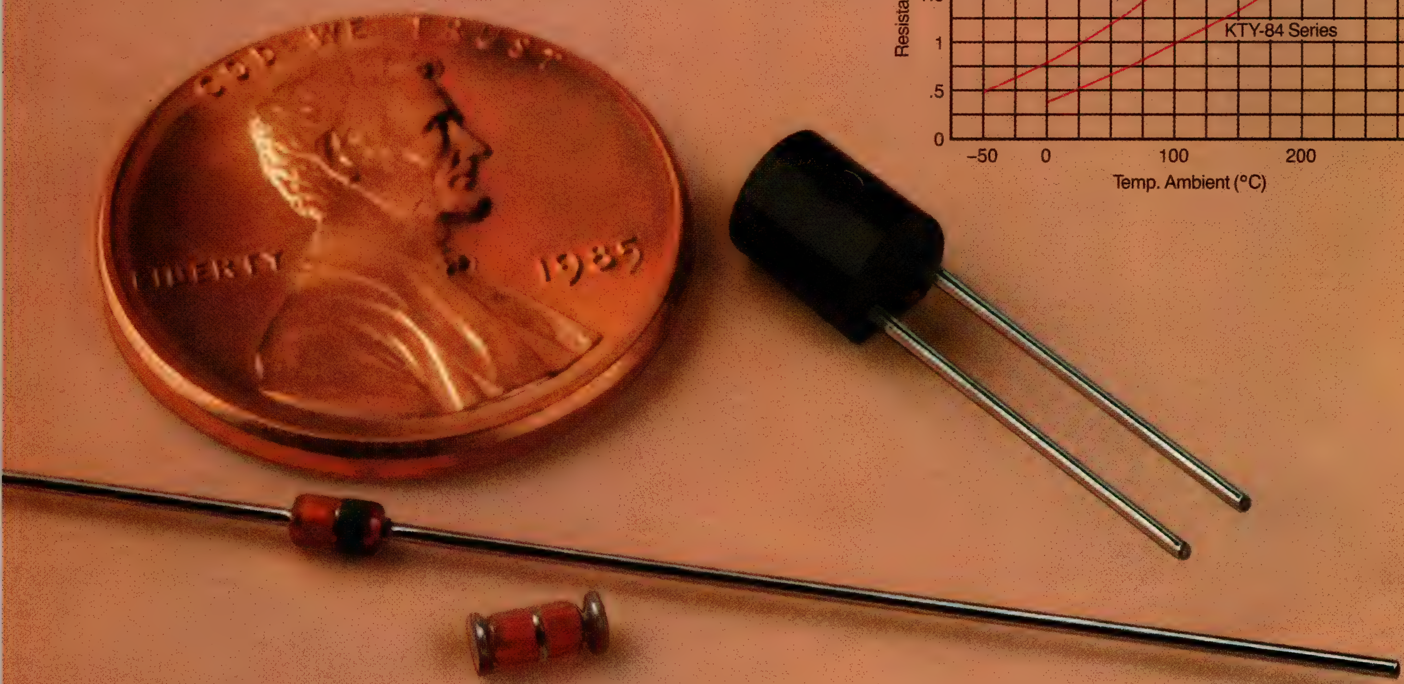


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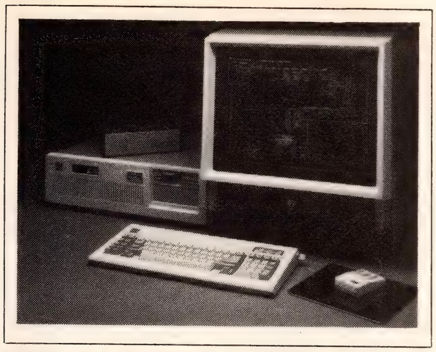

## TEST DEVELOPER

Personal Testmaster is identical to this company's Testmaster package, except that this later version runs on the IBM PC/AT. (The original package runs on the company's own CAE workstations.) The software comprises three tools: a testability analyzer, a fault simulator, and a tester interface. The testability analyzer helps gauge the testability of a design that is still in schematic form. The fault simulator measures the fraction of your design that your test vectors can probe. The tester interface develops conversion programs between the CAE workstation and automatic test equipment. $5000.

**Daisy Systems Corp,** 700 E Middlefield Rd, Mountain View, CA 94039. Phone (415) 960-0123.

**Circle No** 350

## CIRCUIT SIMULATOR

Spice Plus, a version of the Spice 3 simulation software, which was introduced last November by the University of California at Berkeley, adds simulations for temperature effects on components that are critical to effective analog designs. The enhanced version also lets designers use op amps by specifying parameters from data sheets. (The package is written in C.) You can complete transient analysis in approximately half the time required in the 2G.6 version. The package also includes four new device models: a MOSFET model designed to overcome short-channel deficiencies in MOSFET simulations, a model for a uniform distributed RC transmission line, and semiconductor resistor and capacitor models. An improved version of the Boyle op amp is included. Spice Plus, $14,500.

**Analog Design Tools Inc,** 66 Willow Pl, Menlo Park, CA 94025. Phone (415) 328-0780.

**Circle No** 351

## MICROVAX-BASED CAD

This workstation for pc-board design combines a MicroVAX I or MicroVAX II and a Ramtek display. It includes software for pc-board layout. The 19-in. display has a resolution of 1280×1024 pixels. The display operates on a DMA parallel interface directly from the MicroVAX. Optional display interfaces include both GKS and Tektronix 4125 emulation. A keyboard and mouse are included; 4-plane display and 16 colors are also standard. The software features 45° autorouting, two types of routers, and schematic capture. From $45,000.

**Vectron Graphic Systems Inc,** 4401 Great America Parkway, Santa Clara, CA 95054. Phone (408) 980-1180.

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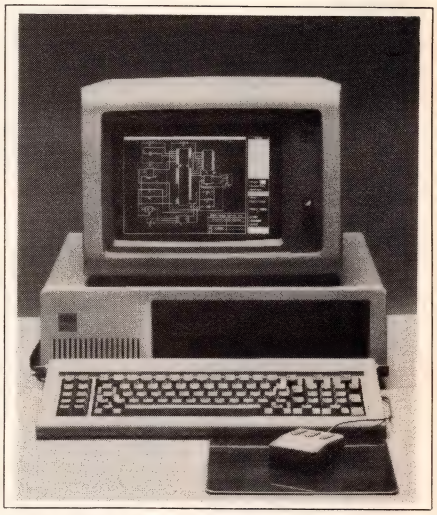
## BUS SIMULATOR

A bus simulator can interface DEC's VAXBI interface chip (BIIC) to the Scaldsystem logic simulator through either the Realchip modeling system or the Realmodel system-level simulation system. (VAXBI is the bus architecture of a family of VAX computers from DEC.) The bus simulator consists of a Realchip adapter board and the files necessary for evaluating the simulation. This vendor sells the adapter board and the software files for $1000; the BIIC, which plugs into the adapter board, is available from DEC.

**Valid Logic Systems Inc,** 2820 Orchard Parkway, San Jose, CA 95134. Phone (408) 945-9400. TLX 3719004.

**Circle No** 353



## PC-BOARD CAD

Dasoft-PC2, CAD software for pc-board design, features a 600-component library. Using the package's graphics editor, you can expand the symbol library. Pin descriptions can include numbers, names, and unit-designation positions. A footprint editor contains six pad shapes; you can define additional pad layouts. The autorouter can interconnect various pad shapes and sizes, including the single-sided pads used in surface-mount technology. The router either can run fully automatically or can obey rules that you specify. The software can lay out schematics and pc boards as large as 160 in$^2$; it automatically scales boards on your screen. The package runs on IBM PC/XTs or PC/ATs that include 512k bytes of RAM, a monochrome graphics card, hard-

disk storage, and a mouse. The software also runs on the AT&T 6300 and the NEC 9801. Hewlett-Packard, Houston Instruments, Western Graphtek, and Ioline plotters can interface to the system. $3495.

**Dasoft Design Systems Inc,** 2550 Ninth St, Suite 113, Berkeley, CA 94710. Phone (415) 486-0822.

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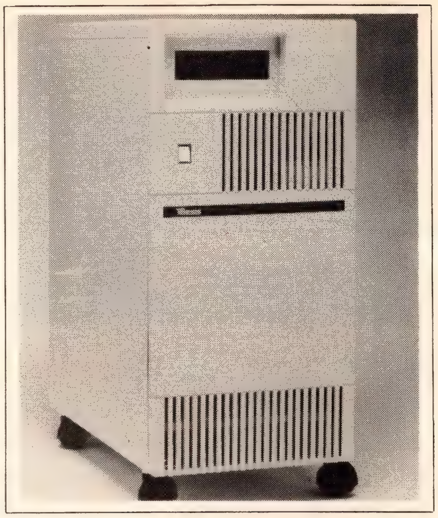

are available as options. Equipped with an Ethernet-based communications link, the accelerator is available to all of the company's other workstations on a given network. You can process multiple serial tasks serially or simultaneously. A digital board, with 613 equivalent ICs and 4414 connections at 0.43-equivalent-IC density, was completed in 7 hours. $47,900. Delivery, 60 to 90 days ARO.

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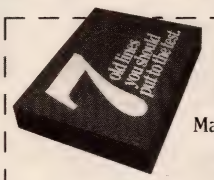


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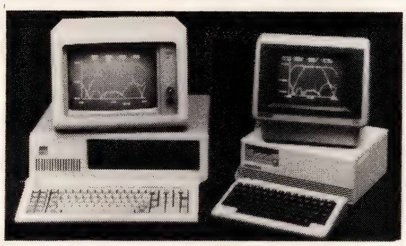
## TTL FUNCTIONS

Softcells, which contains 60 cells that represent TTL functions, is aimed at those design applications where an existing TTL board is being converted into a VLSI application-specific circuit, such as a gate array or standard cell. The software automatically performs the conversion of the TTL/MSI structure to CMOS-process, application-specific IC cells. After the designer has selected the appropriate 7400 Series TTL/MSI function from the company's cell library, the software automatically selects the appropriate cells from the library's database to compose the TTL function. The cells include bus transceivers, synchronous and ripple counters, decoders, multiplexers, and other functions including 4-bit ALUs. Annual license fee, $500 each for standard-cell or gate-array design kits.

**Gould AMI Semiconductors,** 3800 Homestead Rd, Santa Clara, CA 95051. Phone (408) 246-0330.

**Circle No 357**



## LINEAR SIMULATOR

The Touchstone 1.4 linear-simulation program aids in the design, analysis, and optimization of RF and microwave circuits. It provides element models, including asymmetric coupled-microstrip transmission lines, 6- and 8-finger interdigital couplers, a proprietary hole model, a linear taper in microstrip, a microstrip tee junction, microstrip radial line, and other microstrip bend models. The program also features the placement of equations among element values in a circuit, an advanced gradient optimizer, a mouse interface for the tuner and editor functions, and the inclusion of permeability and dielectric and magnetic loss in waveguide and transmission-line models. You can construct circuits using such elements as microstrip, stripline, microwave ICs, waveguides, and substrates. And you can determine parameters such as those for noise, stability, impedance, differential phase shift, group delay, gain and loss, and all S parameters. You can optimize as many as 25 variables simultaneously. The package is available for IBM PC and compatibles, HP Series 200, HP Vectra, and the DEC VAX line. $8400.

**EEsof Inc,** 31194 La Baya Dr, Westlake Village, CA 91362. Phone (818) 991-7530. TLX 384809.

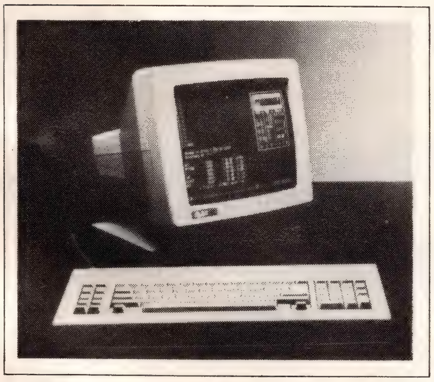
**Circle No 358**

## 256-MIPS CPU

The DataFlo LDF 100 is a real-time processor for such dedicated high-speed applications as signal processing. You can order it in configurations that perform at computational speeds ranging from 5 MIPS to 256 MIPS. To improve the performance of the basic 5-MIPS system, you add modular processors. This computer is based on an architecture that allows the processors to operate only when data is available. This mode of operation solves the timing and coordination problems associated with instruction-driven parallel-processor design, where instructions must be continuously processed. The CPU uses the Genix operating system, a Berkeley implementation derived from Unix under license from AT&T. The manufacturer offers C and Fortran programming languages. From $67,000.

**Loral Instrumentation,** 8401 Aero Dr, San Diego, CA 92123. Phone (619) 560-5888.

**Circle No 359**

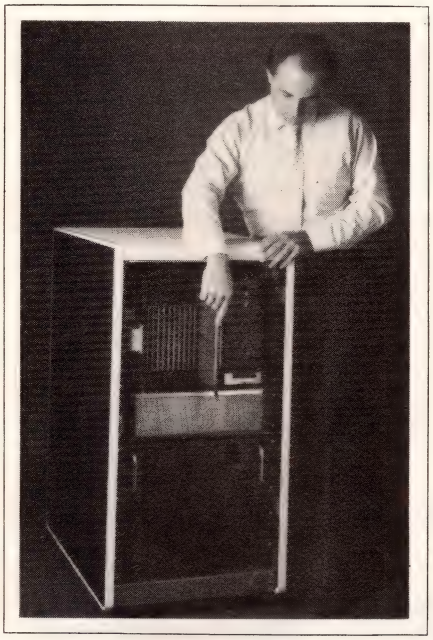


## PC TERMINAL

The Remoterm workstation provides remote access to the IBM PC, PC/XT, PC/AT, or compatible computers and networks. If necessary, this terminal can also furnish remote access to mainframe computers. In addition, you can use the workstation to perform remote PC diagnostics. To start operation, you load the workstation's operating software into a remote PC. Then you either directly connect the two machines or use a modem. The terminal includes a 14-in. green or amber CRT that produces 80- and 132-column displays in a 9×14-dot matrix. You can adjust or detach the keyboard, which has an IBM PC/AT layout. The terminal has two RS-232C bidirectional ports that you can configure as host ports or as serial printer ports. $699.

**Link Technologies Inc,** 47339 Warm Springs Blvd, Fremont, CA 94539. Phone (408) 943-0143.

**Circle No 360**

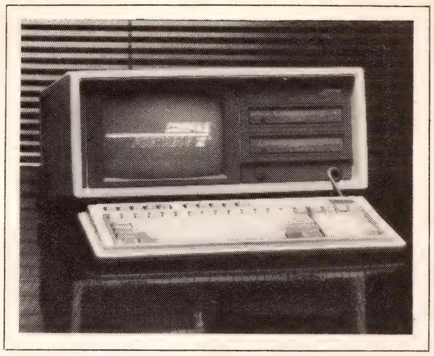


## ELECTRONIC DISK

The RAMdisk/3200 increases the performance of a Perkin-Elmer 3200 mainframe. By adding as much as 128M bytes of solid-state memory, the device can improve data I/O and program access times in a manner transparent to your software. You can order it in a rack-mounted chassis version with 8M to 32M bytes of RAM, or in a stand-alone cabinet version that contains from 24M to 128M bytes of RAM. The latter model contains a battery-backup power supply. From $14,498.

**Zitel Corp,** Performance Systems Group, 399 W Trimble Rd, San Jose, CA 95131. Phone (408) 946-9600. TWX 910-338-0567.

**Circle No 361**



## PORTABLE COMPUTER

This full-function 80286-based personal computer, the Portable II, is an IBM PC/AT-compatible computer that runs software three to five times faster than the 8088-based PCs can. The computer weighs 23.6 lbs and measures 7.5×13.9×17.7-in. Standard features include a 9-in. dual-mode monitor, real-time clock, serial and parallel interfaces, monitor interfaces, and an 84-key keyboard with top-mounted function keys. The case can accommodate two mass storage devices: either two 360k-byte 5¼-in. floppy-disk drives or one floppy-disk drive and one 10M-byte hard-disk drive. The unit also has two expansion slots; you can configure the computer with a maximum of 4.1M bytes of RAM. From $3499.

**Compaq Computer Corp,** 2055 FM149, Houston, TX 77070. Phone (713) 370-0670.

**Circle No 362**

## BUSINESS SYSTEM

The 3000 Series 70 computer offers 20% to 30% better performance than the 3000 Series 68 μCs. It includes as much as 16M bytes of main memory and as much as 128k bytes of cache memory. This optimized memory-access time results

in faster system operation. A basic system includes 8M bytes of RAM, two I/O channels, and necessary operating software. The software package includes MPE V/E, TurboImage/V, KSAM/V, and a number of system utilities. A file upgrade is available for the 3000 Series 68 system. The options package includes a 404M-byte disk drive, 6250-cps tape drive, and a system console for $210,750. Basic system, $150,000; file upgrade, $30,000.

**Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

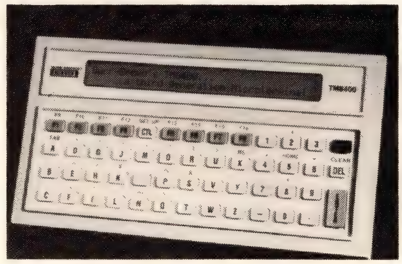
**Circle No 363**

## PORTABLE RAM


Featuring a storage capacity that ranges from 256k to 1.536M bytes of dynamic RAM, the 757 Bytebank is a µP-based data recorder and retrieval unit for either stationary or portable use. An ac power source and battery charger comes with the unit, but its internal batteries let you collect data and load programs for periods as long as 90 hours before recharging. You can program the unit for I/O-interface characteristics, data-communications protocols, error checking, and automatic operation. You can also program the RAM to simultaneously record data and transmit its memory contents to another location via a modem. Other features include a Centronics-compatible printer port and an alarm sensor. From $995.

**Techtran Industries Inc,** 200 Commerce Dr, Rochester, NY 14623. Phone (716) 334-9640. TWX 510-253-3246.

**Circle No 364**




## SMALL TERMINAL

Measuring 9×5×1½-in. and weighing 1.7 lb, the TM8400 is a terminal designed for use in factories. The unit's function keys and user prompts let you establish baud rate, protocol, and other parameters, which the unit then stores in local, battery-backed memory. The unit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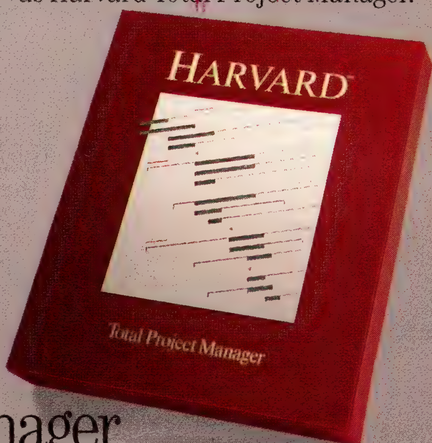


## Graduate to Harvard Total Project Manager

Runs on IBM PC, Compaq, Leading Edge, AT&T and other compatible MS DOS computers. A product of Software Publishing Corporation.

**CIRCLE NO 161**

has a backlit, 2-line×40-character LCD and a 51-key elastomeric keyboard. You can redefine the keys or rearrange the keyboard's physical layout. For expanding the terminal's capabilities, three plug-in modules are available: The communications module enables the TM8400 to operate with RS-232C, RS-422, or current-loop host interfaces. The peripheral module can accommodate a bar-code reader, a magnetic-stripe reader, or a laser scanner. The auxiliary module offers an additional RS-232C port or TTL I/O. TM8400, $745; modules, from $125.

**Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

**Circle No 365**



## EPROM STORAGE

If you have an HP-41 handheld computer, you can use the CMT-10 EPROM plug-in modules to develop custom ROMs. You can reprogram these UV-EPROMs repeatedly and thus avoid the production problems associated with preparing a ROM mask. The modules are available in 4k-, 8k-, and 16k-word versions. A fourth version, the CMT-10-16KB, offers bank switching to double the port memory capacity of your HP-41. With your programs stored in the module, the HP- 41's memory then becomes available for data storage. User-code programs stored in a CMT-10 module will run from 10% to 25% faster than programs stored in the HP-41's memory. To program these modules, you need the CMT-10-F01 EPROM programmer and a computer. Plug-in modules from $95; F01 programmer, $495.

**Corvallis Microtechnology Inc,** Dept 10-B, 33815 Eastgate Circle, Corvallis, OR 97333. Phone (503) 758-3055.

**Circle No 366**

## MODEM

The Model 1224 is a full-duplex, 2-wire 2400-bps modem that solves the problem of errors creeping into a data communications link, according to the manufacturer. Transmitting either synchronous or asynchronous data, the 1224 detects errors and retransmits blocks, al-

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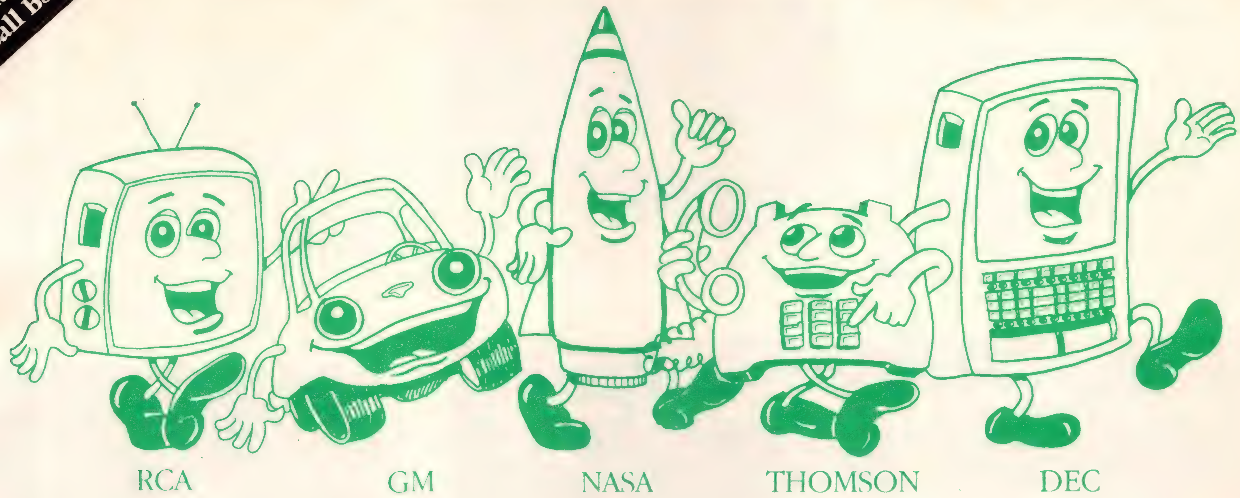


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**BSO UK**
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though this feature is not available if the remote modem does not have the same data-recovery capability. However, the 1224 can automatically detect whether the remote modem has this capability, and will complete handshaking in automatic mode in either case. The 1224 has 12 LED status indicators, 18 switches for parameters on its rear panel,

and three modular jacks for connection to your telephone line, your telephone, and a private line. The unit also features a speaker with a front-panel volume control. $649.

**Case Communications Inc,** 2120 Industrial Parkway, Silver Spring, MD 20904. Phone (301) 381-2300. TWX 710-825-0071.

**Circle No 367**



## MIL-SPEC PRINTERS

The APP-20MIL and APP-48MIL panel-mount thermal printers comply with MIL-STD-202E and MIL-STD-810c. These military-grade printers have a standard operating range of −20 to +50°C. You can choose from parallel, RS-232C, 20-mA loop serial, or IEEE-488 interface. The APP-20MIL provides 20-column printouts and uses 115/230V ac or +12V dc; optional extended temperature range models and a variable power supply are available. The APP-48MIL produces 48-column printouts and has a 12V dc power supply. Both printers offer upper- and lower-case characters and print the entire ASCII 96-character set. The APP-48MIL model supports a second 96-character set of scientific and math symbols. APP-20MIL, $1295; APP-48MIL, $1805. Delivery, six weeks ARO.

**Datel,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-9341. TWX 710-346-1953.

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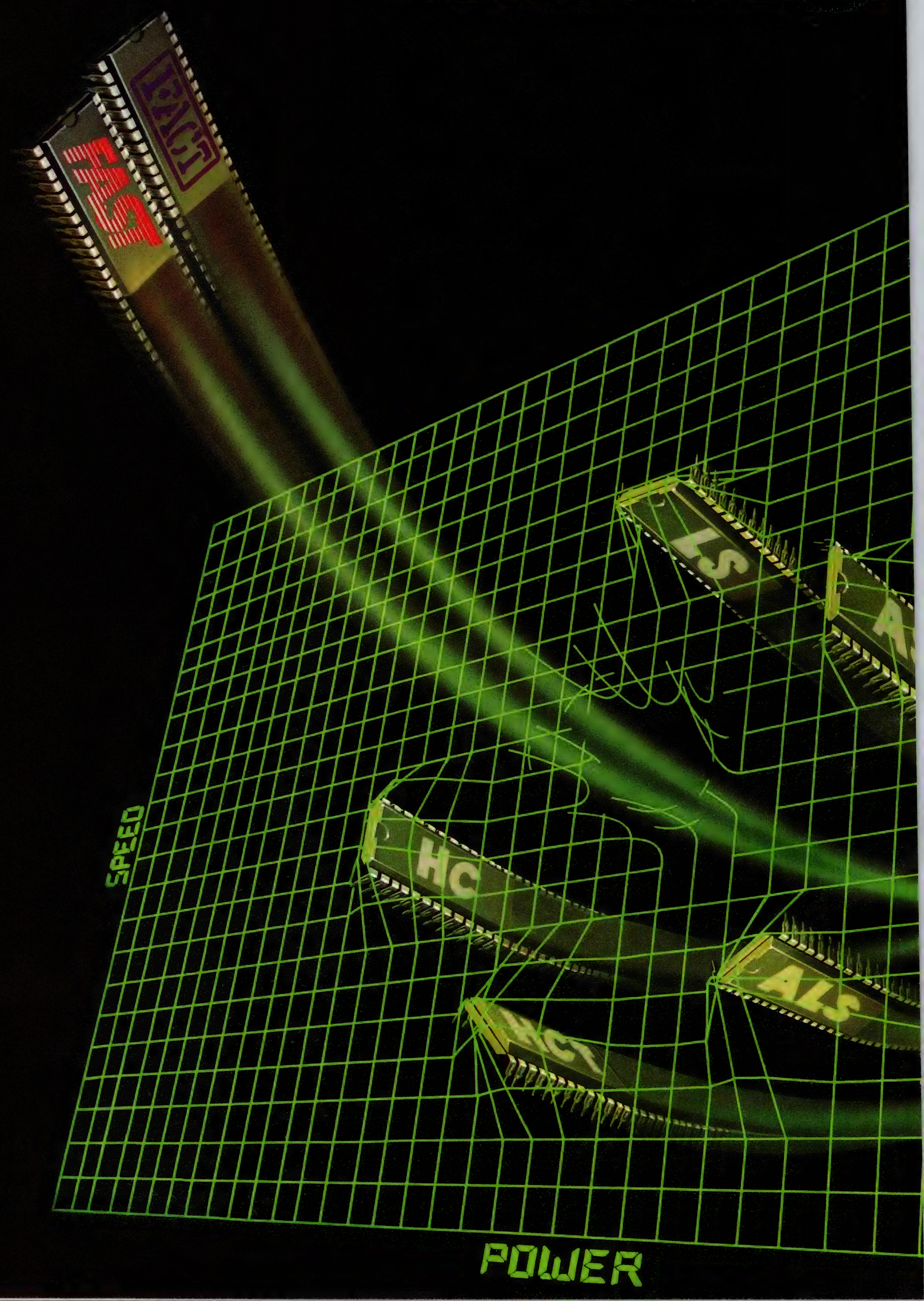

# Oliver Germanium, The Great Detector.

Who'd have guessed it?

It's good old Germanium, after all these years of faithful service, that turns out to be the ideal material for photodetectors, as used in fibre optics and various infrared applications. With Germanium in your diodes, you get the kind of spectral response you've been asking for, (800 to 1800 nm, peaking at 1.550 nm; see curve).

Oliver O. Ward, President of
and frequently referre
as Oliver Germanium,
discovers a fascinatin
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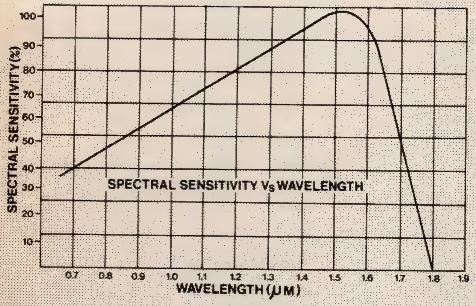



In fact Germanium is especially suited for the 1300 nanometers responsivity required for fibre optics.

Whereas, Silicon as everybody knows, gives very little response beyond 900 nm.

At GPD, we are now making photodiode chips from 0.3 to 5 mm active diameter; all are available either in chip form or in TO-18, TO-5 or TO-8 packages, with windows or lenses to suit the application.

You can use GPD photodiodes in voltaic or conductive modes; to measure optical power or fibre attenuation, and in dozens of other ways.

"The chap we're looking for" said the Great Detector, "is a committed engineer, with a light measurement problem, and a healthy respect for efficient, reliable components."

"I predict the next thing he'll do is send for the GPD photodiode data sheet; then we've got him."

"Elementary, my dear Schottky."

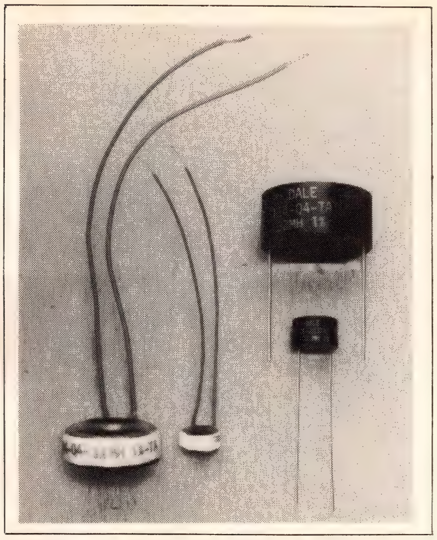
**CIRCLE NO 143**

## Germanium Power Devices Corporation

**Australia** Eastern Crest (Pty) Ltd., 21 Shierlaw Avenue, Room 4, Canterbury, Victoria 3126. Tel: (03) 836 6818. Tlx: 790-38783 EAST. **Austria** Omni Ray GmbH, Vertriebsbüro Wien, Prinz Eugen-Strasse 36, A-1040 Wien. Tel: 0222-65 64 31. Tlx: 132712 omray a. **France** Davum, Dept TMC, 11 Rue Racine, PO Box 28, 93121 La Courneuve. Tel: 836-84-01. Tlx: 210311F (PUBLI). **Sweden, Norway, Denmark and Finland** C.R. Hintze AB, Vasavägen 76, S-18141 Lidingö, Sweden. Tel: 08-767 90 40 Tlx: 10896 chintze s. **Switzerland** Omni Ray Industriestrasse 31, CH-8305 Dietlikon, Tel: 01-835 21 11. Tlx: 53239 omni ch. **West Germany** Protec GmbH. Margreider Platz D8012 Ottobrun. Tel: 089-6097001, Tlx: 529298. **UK Agent** Micron Semiconductor Ltd., 1 Royal Buildings, Marlborough Road, Churchill Industrial Estate, Lancing, Sussex BN15 8UN. Tel: 0903-755252. Tlx: 877698 FLORAK. **UK Distributor** Rofin-Sinar Laser UK Ltd, 2-3 Waterside, Hamm Moor Lane, Weybridge, Surrey KT15 2SN Tel: 0932-58566 Tlx: 8952671 SINUK.

GPD Box 3065, Shawsheen Village Station, Andover, Mass 01810.

Telephone: (617) 475-5982. Telex: 94-7150 GPD Andr.



## TOROIDAL INDUCTORS

Available in pc-board-mountable (Model TE) and leaded (Model TD) styles, these toroidal inductors span a range from 50 μH to 20,000 mH and can be ordered in tolerances of 1, 2, or 5%. Model TE meets MIL-T-27 (type TF5SX20ZZ) and has tinned copper leads. Its body is encapsulated in epoxy. The commercial Model TD has Teflon-insulated leads of stranded tinned copper. A nonflammable vinyl coating protects its winding. A typical commercial style with an inductance range from 50 μH to 10 mH costs $3 (1000).

**Dale Electronics Inc,** 2064 12th Ave, Columbus, NE 68601. Phone (605) 665-9301.

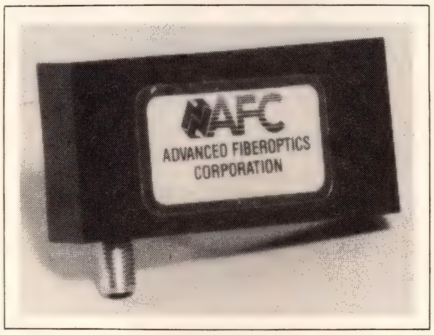
**Circle No 369**

## LCD BAR GRAPHS

The Series 2020-1×41 LCD bar graphs feature a 40-bar display plus a zero bar reading. Resolution is 2.5%. Separate annunciators display negative-input, overrange, and hold functions. You can display the bar graph in either full-bar or individual-bar mode. Two sizes are available: The Model 2020-1×41-1 has an overall glass size of 2.45×1.2 in. and bars measuring 0.65×0.025 in. The Model 2020-1×41-2 has a glass size of 4×2 in. and bars measuring 1.3×0.05 in. Both units have 0.1-in. contact centers. You can use elastomeric strips or pin configurations for connection. Operating range is −40 to +85°C. Units are available for horizontal or vertical mounting. A 5V supply is required for battery applications. Normally clear and normally dark displays with multiple colors are available. 2020-1×41-1, $9; 2020-1×41-2, $24 (1000).

**UCE Inc,** 24 Fitch St, Norwalk, CT 06855. Phone (203) 838-7509.

**Circle No 370**




## F-O MODULES

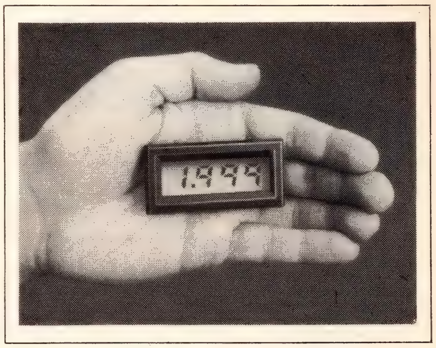
Links built with the AFDR-2000 fiber-optic receiver and the AFDT-2000 fiber-optic transmitter operate at speeds to 50M bps (nonreturn to zero) and provide a worst-case link margin of 20 dB when used with 50-μm-core, graded-index fiber cable. Both the receiver and transmitter mount on pc boards and are TTL compatible. The modules have an operating wavelength of 850 nm and support transmission distances to 5 km or more. Available versions of the modules provide pigtail or SMA optical interfaces. The components require ±5V dc and are designed to operate over 0 to 70°C. AFDR-2000, $150; AFDT-2000, $225.

**Advanced Fiberoptics Corp,** 637 S Haydon Rd, Tempe, AZ 85281. Phone (602) 966-0323.

**Circle No 371**

## PANEL METERS

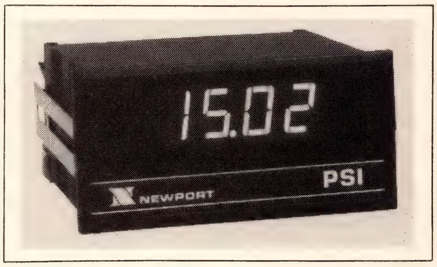
The DP-600 Series 3½-digit LCD digital panel meters feature low-noise differential inputs, automatic zeroing, 0.1% basic accuracy, and automatic polarity indication. Mod-



els are available with input voltage ranges of ±200 mV dc, ±2V dc, and ±20V dc. Input impedance can reach 1000 MΩ, input bias current is 1 pA typ, and common-mode rejection is 86 dB. An onboard low-drift voltage reference is provided; however, the connection of an external voltage reference when required is also possible. All models are packaged in 2.3×1.1×0.4-in. bezel-mount cases. Power requirement is 5V dc at 15 mW. Temperature range is 0 to 50°C. $39 (100).

**Acculex,** 1 Exeter Plaza, Boston, MA 02116. Phone (617) 267-0800. TLX 240713.

**Circle No 372**



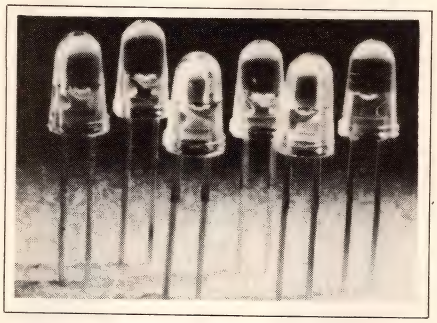

## PROCESS MONITOR

The Model 202-P is a 3½-digit process monitor for signals that require zero and span adjustments, such as 4 to 20 mA, 1 to 5V dc, and 0 to 10V dc. Standard features include a screw-terminal barrier strip for signal and power, and true-differential signal input for common-mode noise rejection of 120 dB. The display span is ±1999 counts and accuracy is 99.9%. The unit fits a standard ⅛-DIN panel cutout and requires a depth of <104 mm behind the panel. Options include a splash-proof lens cover, which provides protection to NEMA-12 standards in industrial

environments. The required external reference voltage can be derived from the meter's 5V dc supply. $164.

**Newport Electronics Inc,** 644 E Young St, Santa Ana, CA 92705. Phone (714) 540-4914.

**Circle No 373**



## BIPOLAR LEDs

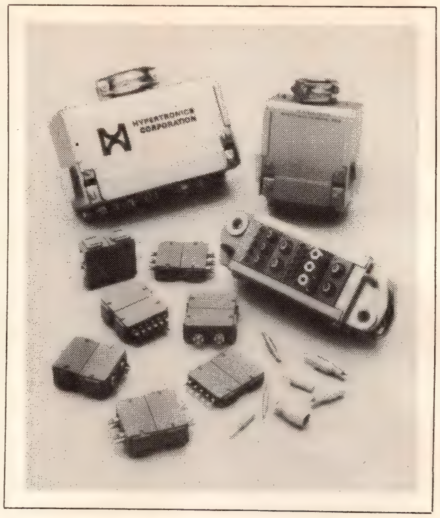
The Series 4301H1/1 and 4301H5/5 bare LED indicators, each incorporating two parallel LED chips of opposite polarity, will operate properly regardless of the polarity of the applied dc. The LEDs do not require the use of external rectifier diodes: They are self-protected. The 4301H1/1 produces a red-light output with either polarity; the 4301H5/5 generates a green-light output with either polarity. The units are T-1¾ LEDs with viewing angles of 50°. Luminous intensity is typically 2 mcd for the red and 14 mcd for the green for 20-mA drive current. Either model, $0.54 (1000).

**Industrial Devices Inc,** 7 Hudson Ave, Edgewater, NJ 07020. Phone (201) 224-4700.

**Circle No 374**

## CONNECTORS

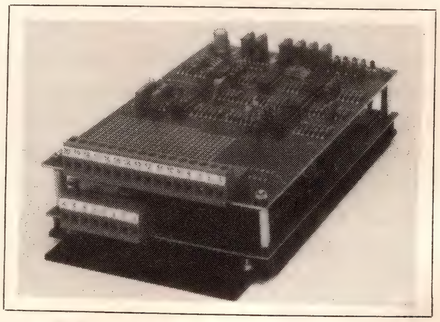
The L Series connectors provide standard modules with signal, power, high voltage, and coaxial contacts. Standard frames and mountings allow packaging for rack-and-panel, cable-to-chassis, and programming applications. The Hypertac contact provides low insertion force and furnishes a life of nearly 100,000 cycles. Contacts position range from 2 to 17 with cur-




rent ratings from 5 to 50A. Module range from 2 contacts at 5A to 17 contacts at 5A. $20 to $80. Delivery, eight to 10 weeks ARO.

**Hypertronics Corp,** 16 Brent Dr, Hudson, MA 01749. Phone (800) 225-9228; in MA, (617) 568-0451.

**Circle No 375**



## SERVO AMPLIFIER

The Amp/10/70 servo amplifier provides 10A continuous and 25A peak at 70V; it has better than 95% efficiency at rated current and requires no external heat sink. The switching frequency of this PWM amplifier is 20 kHz. The amplifier operates in either a voltage or a current mode. It accepts a ±10V-range input command, so you can directly interface it to commercial motion controllers. The output has better than 0.5% linearity and zero dead band. In the current mode, bandwidths can range to 2 kHz. A filter eliminates conditional stability in systems with lag compensation. The amplifier is protected against such system faults as voltage irregularities, in-

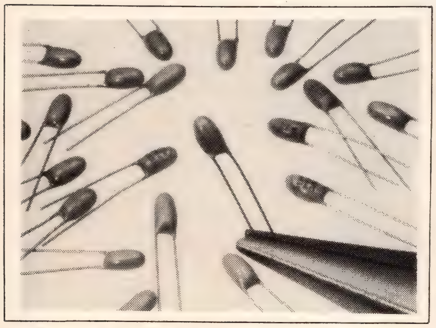
  


IF YOU THINK MEMORIES IS A
CLOSED MARKET, THINK AGAIN.

correct supply connection, excessive temperature, insufficient load inductance, and shorts between output to ground and output to supply. $440.

**Galil Motion Control Inc,** 1928-A Old Middlefield Way, Mountain View, CA 94043. Phone (415) 964-6494. TLX 171409.

**Circle No 376**



## RADIAL CAPACITORS

The Tap Series of solid tantalum capacitors uses the company's tantalum power technology. The housing is flame retardant. Capacitance ranges from 0.1 to 680 μF over 3 to 50V with tolerances of ±20, ±10, or ±5% available. The devices have sintered anodes and solid electrolyte. The series is approved to CECC 30-201-017. Capacitors are available taped on reels or in packs for automatic insertion. $0.065 for 1-μF device with a working voltage of 35V; to $1.55 for 680-μF capacitor with a working voltage of 3V. Delivery, eight weeks ARO.

**Stantel Components Inc,** 636 Remington Rd, Schaumburg, IL 60195. Phone (312) 490-7150. TWX 910-291-1280.

**Circle No 377**

## RTD THERMOMETER

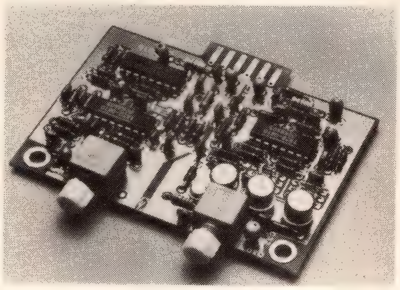

When used with a platinum, 100Ω sensor, the 807 wide-range digital thermometer provides an accuracy of ±0.05% and a resolution of 0.1 or 1°, per customer specification. Sensor-lead-resistance compensation is automatic. A selector switch determines a 3- or 4-wire configuration. Line filtering and 1400V isolation furnish immunity to common-mode signals and high-level noise. Temperature range is −328 to +1472°F for the 1°-resolution model. (The 0.1-resolution option covers a smaller range.) Two optical filters and a switch let you change from Fahrenheit to centigrade. $279.

**Hades Manufacturing Corp,** 151 Verdi St, Farmingdale, NY 11735. (516) 249-4244.

**Circle No 378**



CIRCLE NO 27



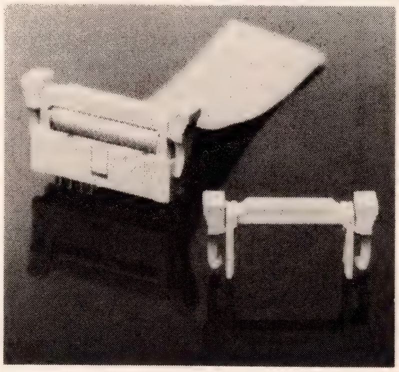
## F-O TRANSCEIVER

The pc-board-mountable HFBR-0422 fiber-optic transceiver comprises the HFBR-1402/1404 transmitter and the HFBR-2404 receiver. It operates with circuitry that can interface with TTL and ECL families. The device is designed for systems that require a 50M-baud data rate and that operate within a 0 to 70°C temperature range. With a minimum optical-power allowance of 12 dB, the transceiver can function in fiber-optic links using HFBR-3000 cable at distances to 2 km. The device requires a 5V power supply. The circuit design and ECL components used on the board also allows the transceiver to function at −5.2V. You can convert the TTL I/O to ECL. $185 (50).

**Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

**Circle No** 379



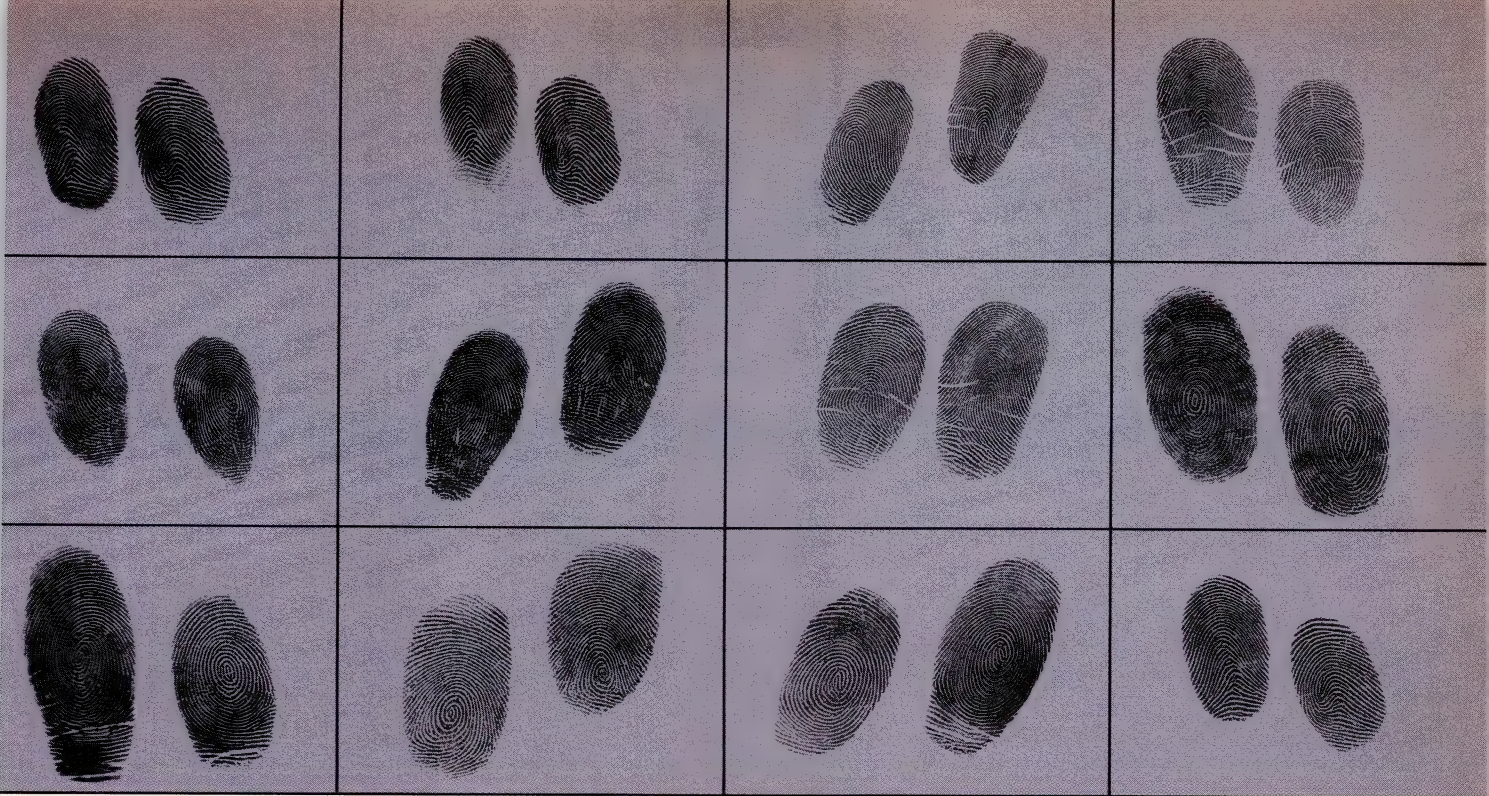


## LOCKING TABS

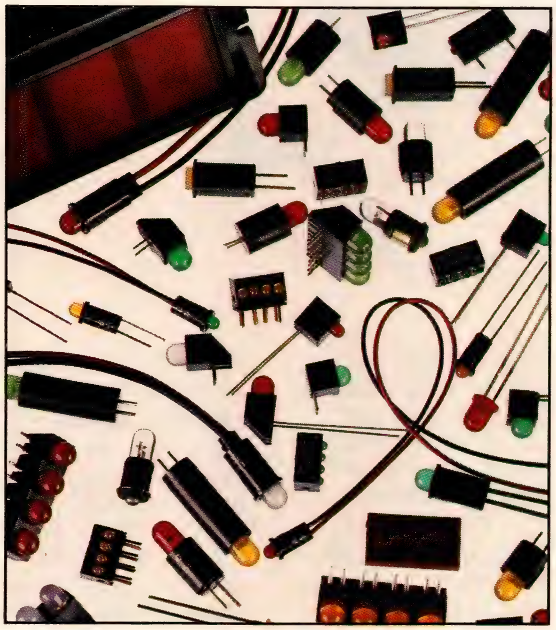
These locking tabs with strain relief caps provide locking of IDC sockets into low-profile headers. The parts are available for 10-, 14-, 16-, 20-, 26-, 34-, 40-, and 50-position headers. These locking tabs also serve as removal tabs. The strain-relief cap attaches to the socket body, not the IDC cover. Molded of glass-filled polyester (UL flammability rating 94V-0), the locking tabs are 0.68 in. high and 0.272 in. wide. Length depends on the number of positions and varies from 0.748 to 2.748 in. You can order tabs separately and snap them into the strain-relief caps. Locking tabs with strain-relief caps, $0.12 to $0.18 (5000).

**Carrot Components Corp,** 750 W Ventura Blvd, Camarillo, CA 93010. Phone (805) 484-0540.

**Circle No** 380



## *BECAUSE NO TWO ENGINEERS ARE EXACTLY ALIKE, DIALIGHT OFFERS THE LARGEST OPTOELECTRONICS VARIETY.*



With everything electronic getting smaller, PC boards and front panels are getting more complicated and difficult to service.

Fortunately, Dialight optoelectronics can help throw some light on the subject. And that's why using this technology is becoming the mark of a good design engineer.

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Suppose you want to backlight a front panel from an internal PC board.

You could use value-added Dialight LEDs. They plug right into the board and hold the light steady at exactly the right distance from the panel.

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Dialight packages LEDs to make them easier to insert. With no need to bend, trim, and possibly break, delicate leads.

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*Products of your imagination.*

**CIRCLE NO 80**

# THE SWITCH IS ON TO EECO FULLY SEALED SWITCHES

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***MICRO-DIP®*** *EECO's* ***subminiature rotary DIP switch*** *measures an incredible .190 inch high and .380 inch square maximum—an ideal data entry device for address encoding or logic line bussing.*

***STRIPSWITCH®*** *Designed for easy use, EECO's* ***low profile PCB-mounted rotary thumbwheel*** *allows you to set or change binary code positions easily with your thumb or through a molded-in screwdriver slot.*

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***Lifetime Warranty.*** *We're so sure our PCB family will withstand the big plunge, we warranty these switches to be free from defects in both material and workmanship for life. And, with engineering and production facilities in the United States and the United Kingdom, you can be sure of on-the-spot technical assistance. Distribution is worldwide, making EECO as near as a local phone call.*

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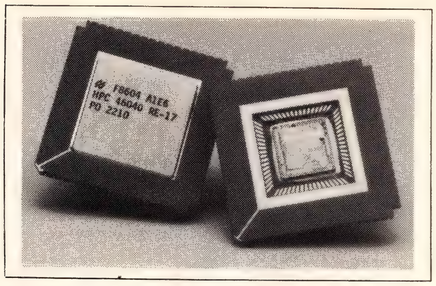
**CIRCLE NO 85**

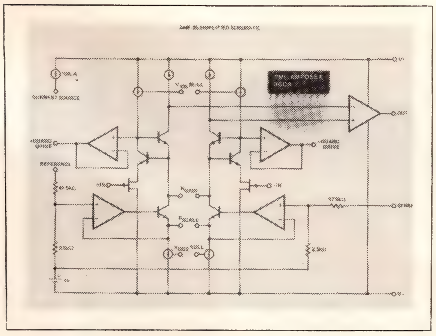


## MICROCONTROLLER

The HPC16040, the first member of the HPC family of microcontrollers, has an instruction cycle time of 240 nsec. The device is a complete microcomputer on a single chip. It includes 4k bytes of ROM, 256 bytes of RAM, 52 I/O lines, eight 16-bit timers (including four pulse-width-modulated timer registers), and an on-chip UART. The device's instruction set includes 16-bit multiply and divide, single-byte jumps and calls, nine addressing modes, and versatile bit-manipulation instructions. All memory, I/O, onboard peripherals, and registers are memory-mapped into the controller's 64k-byte address space. In an industrial-temperature-range (−40 to +85°C), 68-pin plastic leadless chip carrier, $29.90.

**National Semiconductor Corp,** Box 58090, Santa Clara, CA 95052. Phone (408) 721-5926. TWX 910-339-9240.

**Circle No** 381

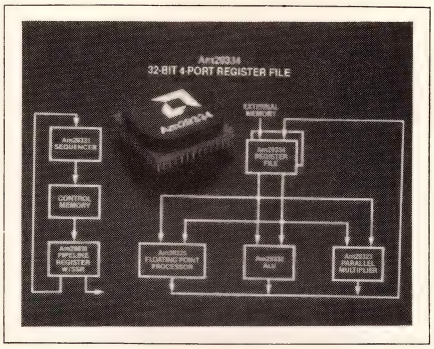


## INSTRUMENTATION AMP

The AMP-05 instrumentation amplifier offers 15-μsec max settling time to 12 bits at gains as high as 2000 and 14-bit gain linearity at G≤1000. The device offers on-board dual guard drivers and a 100-μA precision current source. At 25°C, CMRR is 110 dB min at G=1000. The JFET inputs reduce bias currents to 50 pA max at 15°C and 20 nA at 125°C. The device's output is guaranteed stable with loads as high as 2 nF; the device features a slew rate of 5V/μsec and a 120-MHz gain-bandwidth product with gain set at 1000. In an 18-pin ceramic DIP, $9.90 (100).

**Precision Monolithics Inc,** Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 910-338-0218.

**Circle No** 382

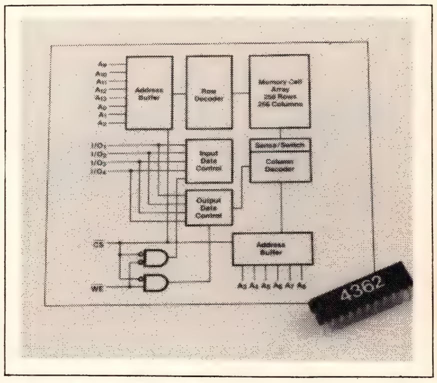


## REGISTER FILE

The Am29334 register file has an access time of 24 nsec and supports an 80-nsec system cycle time when used with the other members of the Am29300 32-bit, bipolar building-block μP family. The device provides two write and two read ports for data and four 6-bit address ports. Two of the address ports access each pair of read and write data ports—one to read data and the other to write—thereby providing two reads and two writes in one cycle. The device is organized as 64×18 bits. It is horizontally and vertically cascadable to support greater word widths and deeper register files, allowing unlimited expandability. A byte-parity storage feature supports the fault-detection scheme of the family of μPs and eliminates errors arising from interconnections. A single-phase lock input simplifies timing for read and write cycles. The byte-write capability allows writing either individual bytes or full words; the IC thus accommodates 8-, 16-, and 32-bit systems. In a 120-lead pin-grid array, $180 (100).

**Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94088. Phone (408) 732-2400.

**Circle No** 383




## STATIC RAM

The μPD4362 64k static RAM features access times of 45, 55, and 70 nsec. The 16k×4-bit organization provides maximum density and flexibility in configuring cache- and buffer-memory systems. The device is implemented in mixed NMOS/CMOS technology, and the memory cells are designed with four MOS transistors and two polysilicon resistors to minimize chip size. The output drivers are designed with 3-state CMOS technology for low power and full TTL compatibility. In a 22-pin plastic DIP, $43 (100).

**NEC Electronics Inc,** Box 7241, Mountain View, CA 94039. Phone (415) 960-6000. TWX 910-379-6985.

**Circle No** 384

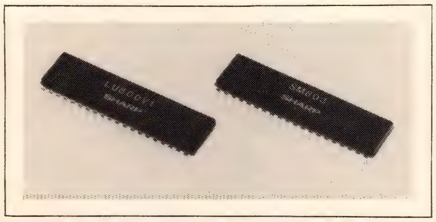
## STANDARD CELLS

Sixty standard cells, called SoftCells, offer standard 74-Series logic functions. Bus transceivers, synchronous and ripple counters, decoders, shift registers, and flip-flops are included in this group of cells. The conversion of the TTL/MSI structure to CMOS-processed, application-specific IC cells is performed automatically by software. These devices target applications where an existing TTL board is

being converted into a very large-scale integrated application-specific circuit, such as a gate array or standard cell. $500.

**Gould AMI Semiconductors,** 3800 Homestead Rd, Santa Clara, CA 95051. Phone (408) 246-0330.

**Circle No** 385



## MICROCOMPUTERS

The SM803 and LU800V1 are 8-bit, single-chip CMOS μCs compatible with their LH0811 and LH0881 counterparts. The SM803 contains 4k bytes of internal ROM. The LU800V1 version has no ROM; you can use it as a development tool for the SM803 or as a stand-alone μC with external ROM. Both devices operate at a speed of 8 MHz max and draw supply current of 12 mA typ at full power, dropping to 2.4 mA in the halt mode and 150 μA in the stop mode. The ICs contain 144 bytes of RAM, a full-duplex UART, two programmable 8-bit counter/timers, and 32 I/O lines. They are available in 40-pin DIPs, 44-pin flat packs, and 44-pin J-bend PLCCs. SM803, $6.71 (5000); LU800V1, $7.43 (1000). Delivery, eight weeks ARO.

**Sharp Electronics Corp,** Sharp Plaza, Mahwah, NJ 07430. Phone (201) 529-8757.

**Circle No** 386

## DARLINGTONS

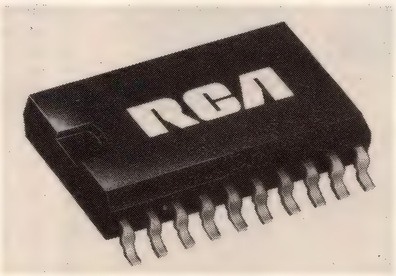
Transipack 1 and 2 are single- and dual-Darlington power-transistor modules containing parallel-connected inverse diodes. Transipack 1 comes in three styles: a single bipo-

lar transistor and single or dual Darlingtons. Rated at 15 to 80A at 800V, the modules are housed in TO-240AA packages. Transipack 2 comes in four styles; ratings are 30 and 50A. A 600V module has a 2-stage Darlington chip; a 1000V device has a 3-stage chip. The devices come with a series connection or a common-emitter connection. Transipack 1 and 2 spec an isolation-

voltage rating of 2500V. You can mount a number of modules on a single heat sink and connect them with bus bars. 50A, 600V Transipack 2, $39 (100).

**Semikron Inc,** Box 66 Hudson, NH 03051. Phone (800) 258-1308; in NH, (603) 883-8102.

**Circle No** 387




## COMPARATOR IC

The CD54/74HC/HCT688 can determine the relative size of two 8-bit binary words. The device comes in two versions: the HC version for CMOS system designs and an HCT version that is compatible with low-power Schottky TTL (LSTTL) bipolar logic. Both versions feature high-speed operation and propagation delay times as low as 14 nsec at 25°C with a 5V supply and 15-pF load. The CD54/74HC operates from 2 to 6V; the CD54/74HCT operates over the TTL supply-voltage range of 4.5 to 5.5V. Both devices operate over −40 to +85°C. The CD54HC comes in a 20-lead ceramic DIP; the CD74HC comes in a 20-lead plastic DIP. $1.24 (100).

**RCA Solid State,** Rte 202, Somerville, NJ 08876. Phone (201) 685-7460.

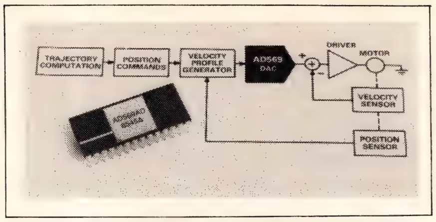
**INQUIRE DIRECT**


## BUFFER

The BB3553 unity-gain buffer amplifier provides high-current drive at frequencies from dc to 300 MHz. The device has a slew rate of 6000V/μsec and can provide 400 mA into a 50Ω load. The design's input requires a bias current of 200 pA at 25°C. Input resistance is $10^{10}\Omega$ min and output impedance is 4Ω max. The device operates over −55 to +125°C and comes in a hermetic TO-3 package. $23 (100).

**Maxim Integrated Products,** 510 N Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 737-7600.

**Circle No** 388

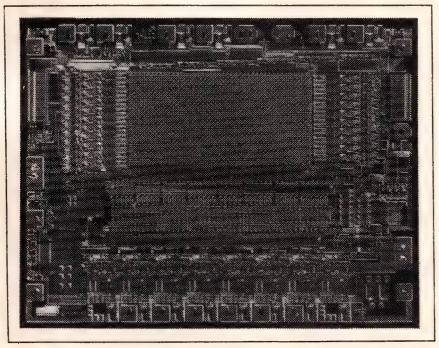



## D/A CONVERTER

The AD569 D/A converter guarantees 16 bits of monotonicity over its specified operating temperature ranges. The device provides direct interface to an 8- or 16-bit data bus. It features 200-mW power consumption, 5-μsec max voltage settling time to ±0.001%, and ±0.01% integral nonlinearity. Force and sense reference terminals reduce gain errors and gain-drift errors. The referenece-input bandwidth is 100 kHz, and ac feedthrough is less than −100 dB. The device comes in five grades: JN, KN, AD, BD, and SD. The JN and KN grades are specified from 0 to 70°C, AD and BD operate from −25 to +85°C, and SD is specified from −55 to +125°C. The device operates from ±12V supplies and comes in a 28-pin ceramic or plastic DIP. $19 (100).

**Analog Devices,** Literature Ctr, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TWX 710-394-6577.

**Circle No** 389



## PLD

The AmPAL18P8 features two additional bidirectional I/O pins for as many as 18 inputs and eight outputs, compared with the 16 inputs and eight outputs typical of other 20-pin PAL devices. Each output has eight product terms and one control term, and you can choose either active-high or active-low states for each one. The device has propagation delays as low as 25 nsec. In a 20-pin plastic package, $3.55 (100).

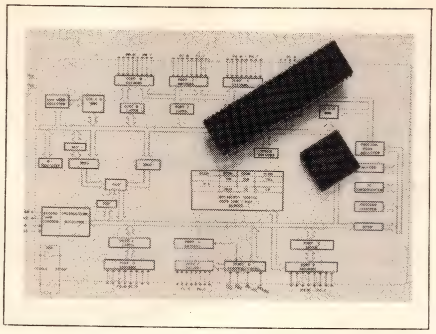
**Advanced Micro Devices,** Box 3453, Sunnyvale, CA 94088. Phone (408) 982-7445.

**Circle No 390**

## MICROCONTROLLER

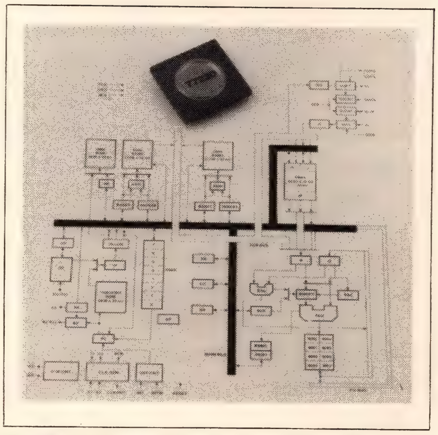
The 83C451 microcontroller is an addition to the company's 8051 family of 8-bit microcontrollers. The device adds 28 I/O lines to the already existing 32 lines. These 60 lines permit designers to eliminate external hardware for address latching, decoding, and data buffering in I/O-intensive applications. Where multi-

ple microcontrollers are needed, the device provides enough I/O to constitute a 1-chip solution. The added I/O takes the pin count to 64 or 68 compared with the 8051's 40 pins. Port 6 consists of eight I/O lines plus four control signals. By programming internal registers, port 6 can be configured for various data-input control and flag operations. The device is fully compatible with the industry-standard 80C51 microcontroller. The device contains a 4k×8-bit ROM and 128k×8-bit RAM. Other features include a 5-source, 2-priority-level nested interrupt structure; serial I/O port for either multiprocessor communications, I/O expansion, or a full-duplex UART; and an on-chip 12-MHz oscillator and clock circuits. In a 64-pin plastic DIP, $20 (100).



**Signetics Corp,** 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000.

**Circle No 391**



## DSP IC

The μPD77230 has on-chip 32-bit floating-point architecture and a 55-bit floating-point multiplier that executes an instruction cycle in 150 nsec. The device can perform a 512-floating-point FFT in 4.7 msec and a 32-tap FIR filter in 5.24 μsec. The device accesses 8k×32 bits of external data and 4k×32 bits of external instruction in one cycle. Multiple internal data paths allow the device to perform a multiply/accumulate, internal data move, and an update of the RAM/ROM pointers in one cycle. The device uses a 5V power supply and has typical power dissipation of 1.7W. In a 68-lead pin-grid array, $260 (100).

**NEC Electronics Inc,** Box 7241, Mountain View, CA 94039. Phone (415) 960-6000. TWX 910-379-6985.

**Circle No 392**

# STEP UP TO E SIZE

Houston Instrument's new E size DMP-56 delivers the precision, throughput, and reliability you require from a drafting-intensive plotter. The DMP-56 also gives you the flexibility to handle 18 different drawing format sizes ranging from 8½ × 11 inches to 36 × 48 inches.

The DMP-56 was designed for any application calling for crisp, clean graphics—whether it's architectural floorplans, mechanical designs, electrical schematics, or overhead transparencies. Because of its media-size adjustment mechanism and automatic media-size sensing feature, the DMP-56 quickly and efficiently responds to your changing format requirements. This high-performance plotter can produce standard (A through E), metric (A4 through A0), oversize (A4 through A0), and Architectural C, D, and E drawings.

The DMP-56 is a professional drafting plotter that draws on the established track record of Houston Instrument's very successful DMP-51/52 and DMP-51/52 MP plotters—plotters that redefined the standard for price, performance, and quality.

Immediately compatible with hundreds of computer-aided design and graphics software packages through our powerful DM/PL™ command language, the DMP-56 also gives you a precise resolution of .001 inch and a maximum plotting speed of 17 inches per second. And, because it uses a standard RS-232-C compatible interface, the DMP-56 can operate with virtually any computer on the market.

The DMP-56 also delivers features you'd expect only from more expensive* plotters—such as quiet servo drive, and an easy-to-use front-panel control. Combine these standard features with the well-known Houston Instrument reliability and support and you have a superior plotter at a reasonable price.

In terms of throughput, performance, price, and quality the DMP-56 is the professional graphics tool you need. For more information, call 1-800-531-5205 (512-835-0900 if in Texas), or write Houston Instrument, 8500 Cameron Road, Austin, Texas 78753. In Europe, contact Houston Instrument, Belgium NV., Rochesterlaan 6, 8240 Gistel, Belgium. Tel.: 32-(0)59-277445. Tlx.: 846-81399.

*U.S. suggested retail price is $5,995. Pricing subject to change.
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CIRCLE NO 93

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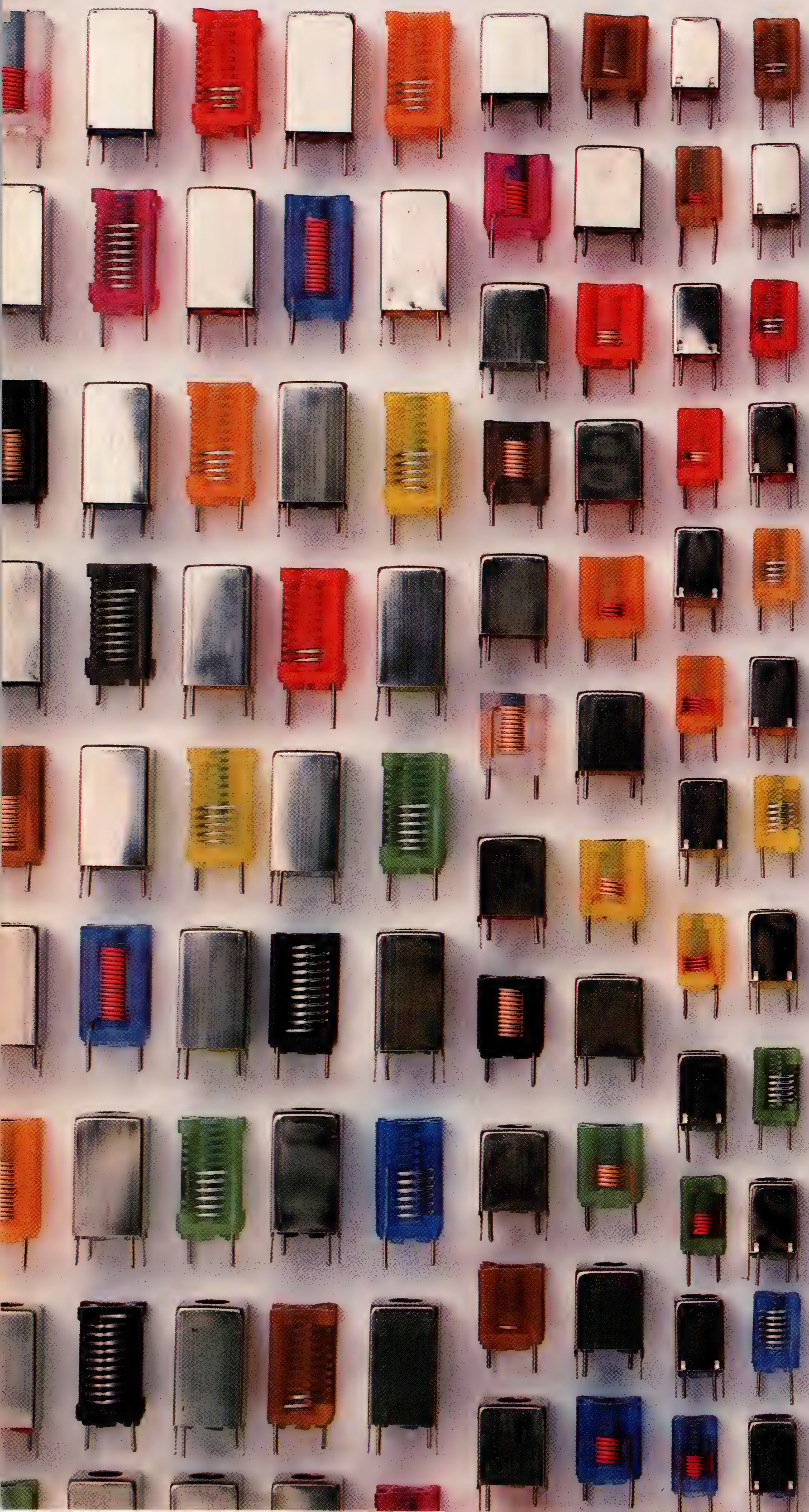

If you need variable inductors in the range from .05 uH to 1100 uH, no one gives you a wider selection than Coilcraft. And no one gives you lower off-the-shelf pricing!

Coilcraft tuneable RF coils are designed to meet MIL specs. They feature compact 10mm or 7mm packaging, optional shielding, and one-piece construction for maximum stability.

For special inductance or Q values, we'll custom-build coils to your specifications and still save you money!

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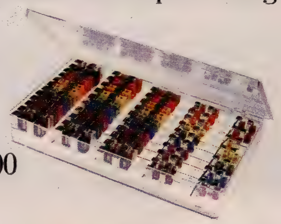
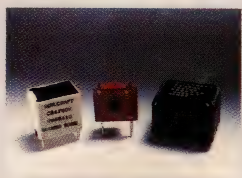
**Experimenters Kits.** Choose kits covering the range from .0425 to 1.5 uH or from .70 to 1143 uH. Kits include shielded and unshielded samples along with detailed specifications. Each costs $60, applied against your first order. Call 312/639-6400 to order.

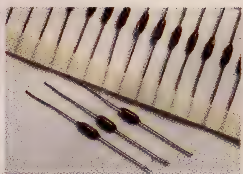


Chip Inductors



Current Sensors

Power Inductors

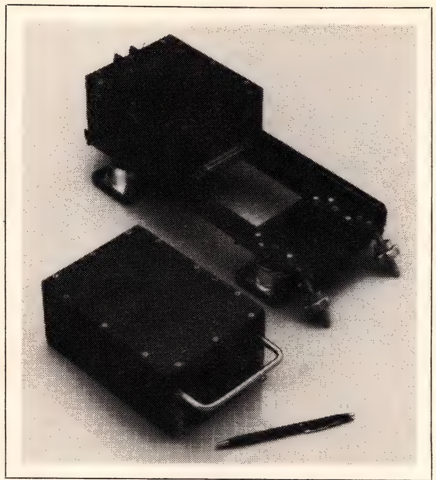


Axial Lead Chokes

Coilcraft

1102 Silver Lake Rd., Cary, IL 60013

CIRCLE NO 76



## HARD DISK

The Model 4100 Small Disk, a 3½-in. Winchester-technology disk subsystem, features 20M bytes of storage on a removable hard-disk assembly (HDA). The HDA is removable for transferring data among systems and for protecting sensitive data. The subsystem weighs 10 lbs, including its hard-disk assembly, power supply, and interface. The subsystem, measuring 3.75×12.6×5.8 in., is packaged in a standard ½-ATR military configuration. When equipped with its optional external shock and vibration isolators, it meets the requirements of MIL-STD-810C for shock and vibration. It contains a SCSI interface. $11,500.

**Rolm Mil-Spec Computers,** 1 River Oaks Pl, San Jose, CA 95134. Phone (408) 942-8000.

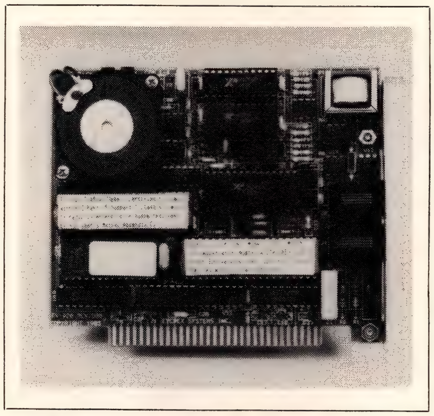
**Circle No 393**

## STORAGE SYSTEMS

The TG Series tape and disk/tape subsystems provide internal storage for various μCs. The TG-1020i, an internally mounted, half-height, 5¼-in. tape drive, backs up 20M bytes of data on one tape cartridge. It is designed for the IBM PC/AT, PC/XT, and compatible computers. The TG-2025i contains a full-height, 5¼-in., 25M-byte hard-disk drive and a 20M-byte tape drive. You can run it in conjunction with the PC/XT and compatibles. Mounted inside the computer, the TG-1425i is a 3½-in., 25M-byte hard disk. Its half-height, 5¼-in. tape drive stores 20M bytes of data on one tape cartridge. This model is compatible with AT&T and Olivetti personal computers. The packages for the three models comprise disk and tape drives (tape drive only for TG-1020i), documentation, the manufacturer's software version 2.0, XTree and Backtrack software, controller, cables, and mounting hardware. Model TG-1020i, $995; TG-2025I, $1995; TG-1425i, $2095.

**Tallgrass Technologies Corp,** 11100 W 82nd St, Overland Park, KS 66214. Phone (913) 492-6002. TLX 437121.

**Circle No 394**

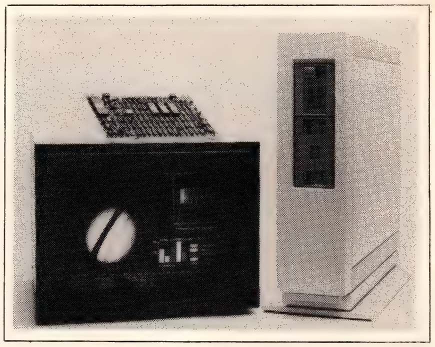


## HALF-CARD MODEM

The Evercom 300/1200-baud modem fits in short slots in the IBM PC/XT, IBM portable, and many compatibles. The Hayes-compatible unit detects incoming transmission rates automatically. The board features call-progress monitoring; voice and data communications; audio and data telephone-line monitoring; half- and full-duplex data transmission; and a built-in loudspeaker. The modem's Bit Com software supports 132-column displays, includes built-in data buffers, and lets you run other programs. A personal dialing directory stores as many as 32,000 phone numbers. $249.

**Everex Systems Inc,** 47777 Warm Springs Blvd, Fremont, CA 94539. Phone (415) 498-1111.

**Circle No 395**

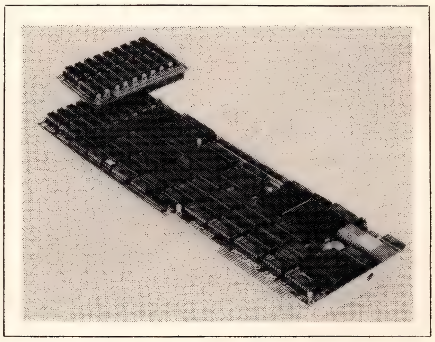


## CONTROLLERS

These two graphics controllers provide medium- and high-resolution graphics to Q Bus computers like the MicroVAX II. The QG-1280 provides graphics resolution of 1280×1024×8 bits and a processing speed of 20,000 vectors per second. It can draw 10,000 cps. The QG-640 offers a resolution of 640×480×8 bits. It contains dual video-output channels, which can be used to support fully independent high-resolution displays with a single board. You can use the onboard graphics code to divide the eight bit planes between the two output channels. Both controllers plug directly into the Q Bus computer. QG-1280, $4995; QG-640, $2995.

**Matrox Electronic Systems Ltd,** 1055 St Regis Blvd, Dorval, Quebec, Canada H9P 2T4. Phone (800) 361-4903; in Canada, (514) 685-2630.

**Circle No 396**



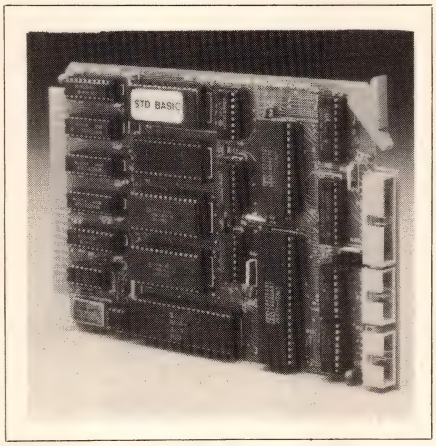
## ACCELERATOR BOARD

Designed to run on the IBM PC and PC/AT, the PCturbo 286e increases system throughput as much as 3.5 times (on an IBM PC). The board contains an 8-MHz 80286 CPU, an 80287 math-coprocessor socket, and

a 16-bit system bus running with no wait states. With an optional daughter board, the accelerator gains 1M byte and thus meets the Lotus/Intel/Microsoft expanded memory specification (EMS). You can also use the extra megabyte of RAM to run programs supporting the IBM PC/AT's extended memory. The disk-caching feature and the RAM disk use PC and Turbo memory to reduce disk access time. A print spooler is also included. PCturbo 286e with 1M byte of factory-installed RAM, $1195; EMS daughter board, $395.

**Orchid Technology,** 47790 Westinghouse Dr, Fremont, CA 95439. Phone (415) 490-8586.

**Circle No 397**

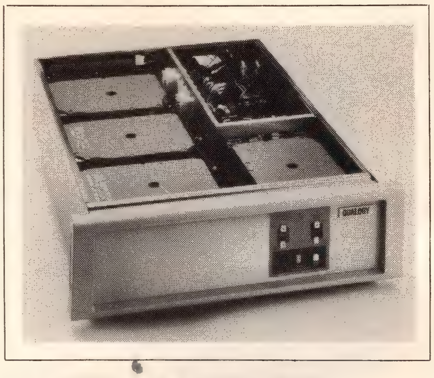



## CPU BOARD

The Octagon 890 multifunction CPU card for the STD Bus incorporates floating-point Basic. Application programs run from EPROM on power up. Forty-four of the 120 commands can directly control systems using bit, BCD, 8-bit, or 16-bit levels. Hardware includes a 4-MHz Z80A processor; dual, independent, RS-232C serial ports; and four 8-bit counter/timer channels. Memory consists of four sockets that can hold 64k bytes of RAM and EPROM. You can address an additional 64k bytes of RAM on the STD Bus. $385.

**Octagon Systems Corp,** 6501 W 91st Ave, Westminster, CO 80030. Phone (303) 426-8540.

**Circle No 398**




## SYSTEM PACKAGES

The three models of the Cyclone Series are compatible with Micro-PDP-11 and MicroVAX operating systems including MicroRSTS and Micro VMS. The D938GL includes one 160M-byte, 5¼-in. Winchester; the D968L combines two 160M-byte hard-disk drives; and the D998GL has four 160M-byte hard-disk drives. These systems are available in rack-mount, table-top, and the company's proprietary MicroPac packaging. The system disks offer access times of 27 msec or less. They feature software diagnostics, automatic power-on tests, and ROM-based diagnostics with a front-panel display readout for off-line diagnostics. D998GL, $22,395.

**Qualogy,** 2241 Lundy Ave, San Jose, CA 95131. Phone (408) 946-5800. TLX 4993489.

**Circle No 399**

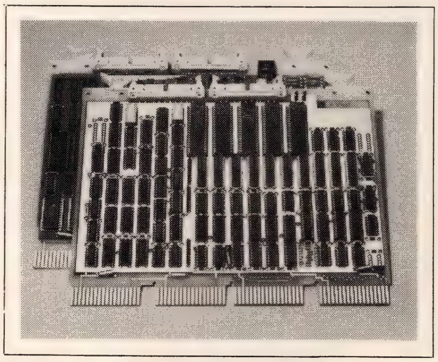
## PC-TO-MINI LINK

The Ideacomm 5251, a twin-axial emulator, links IBM PCs, PC/ATs, PC/XTs, and portable PCs to IBM System 34/36/38 minicomputers, using 50k bytes of system memory. It supports IBM's file-support utility, file-transfer facility, PC Support/36, and PC Support/38. It offers emulation for the IBM 5219, a printer used in IBM System 3X. You can also configure it for printer support emulating IBM 5256 Model 1; 5224 Model 1, and 5225 Model 1 printers. The emulator can also configure IBM's Wheelprinter, HP's Laserjet and NEC's 3550 printers for 5219 emulation. The printer-con-

trol menu displays the printer's status. The board provides as many as four concurrent host sessions (including one printer session) and one DOS session. Besides providing emulation for the IBM 5251 Model 11, 5291 Models 1 and 2, and 5292 Model 1 terminals, the unit can also work with either the IBM color or monochrome display. It can communicate directly to the IBM 3X host computer or via IBM 5251 Model 12 or 5294 remote controllers. 5251 card and software, $895.

**IDEAssociates Inc,** 35 Dunham Rd, Billerica, MA 01821. Phone (617) 663-6878. TLX 948245.

**Circle No 400**



## BUS-CONTROL UNIT

The BCU-11LB, a bit-slice μP-based data-bus interface unit, is compatible with the DEC LSI-11 and with the MIL-STD-1553B bus. It can operate as a bus controller, remote terminal, bus monitor, or bus analyzer on the 1553B bus. Functioning as a controller or remote terminal, the unit can also perform data transfers between remote terminals. It can simulate as many as 32 remote terminals. You can implement all message formats and mode codes specified in MIL-STD-1553B. Other features include DMA, programmable interrupts, and built-in diagnostic self-test. $7150 (10). Delivery, stock to 60 days ARO.

**SCI Technology Inc,** Box 4000, Huntsville, AL 35802. Phone (205) 882-4800. TWX 810-726-2234.

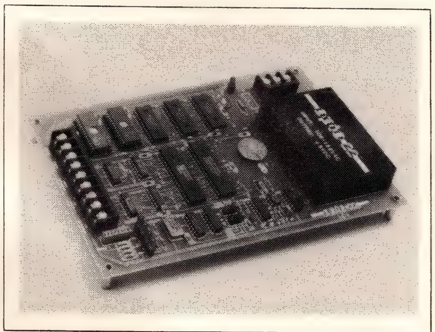
**Circle No 401**

## PC COPROCESSOR CARD

The 32-bit DS-32 PC coprocessor board can run Unix System V and virtual MS-DOS simultaneously, while MS-DOS is running on the PC. The IBM PC-compatible board provides VAX-level performance with full 32-bit data paths on a PC via the 10-MHz NS32032 running with no wait states. As much as 2M bytes of onboard memory is available; with an add-on board, you can have as much as 4M bytes of additional memory. Virtual MS-DOS adds demand-paged virtual memory capabilities to MS-DOS, thereby enabling the PC to run tasks requiring 15M bytes of memory. An optional Unix V.2 also supports virtual memory. The board fits into one slot on any IBM PC or compatible. The unit includes the NS32081 hardware floating-point accelerator, two serial ports, a 16-bit interrupt-driven counter/timer, and an optional NS32082 memory-management unit. From $2500 for a 10-MHz, 1M-byte system.

**Oasys,** 60 Aberdeen Ave, Cambridge, MA 02138. Phone (617) 491-4180.

**Circle No 402**

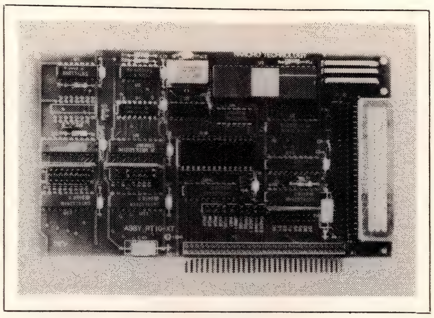


## CONTROLLER

The LC2, a Z80B-μP-based industrial controller, features line-voltage spike suppression, a 70°C ambient operating temperature, brown-out protection, and battery-backed memory. Its IBM PC-compatible drivers facilitate the development of application software. Use of Basic or Forth control languages eliminates ladder-logic programming. You use an RS-422/485 bus throughout the system. $595.

**Opto 22,** 15461 Springdale St, Huntington Beach, CA 92649. Phone (714) 891-5861.

**Circle No 403**



## HOST ADAPTER

The RT10-XT connects SCSI peripherals to the IBM PC/XT and compatible systems. It functions both as an initiator and as a target. It also performs synchronous and asynchronous data transfers and meets ANSI SCSI specification X3T9.2. Its features include PIO/DMA operation, selectable DMA channels, selectable interrupts, a ROM-option socket, and selectable board address. A SCSI application exerciser is also included. <$100 (OEM qty).

**Rancho Technology,** 10238 Monte Vista, Rancho Cucamonga, CA 91701. Phone (714) 987-3966.

**Circle No 404**

## MEMORY CARD

The MVXII is an 8M-byte add-in memory card offering 8192k bytes of additional memory for the MicroVAX II. (You can configure the MicroVAX II to address as many as 16M bytes of memory.) This card implements parity checking and other memory-system features of the MicroVAX II and an on-line/off-line switch, an activity indicator, and a power-on LED. $6500.

**EMC Corp,** 12 Mercer Rd, Natick, MA 01760. Phone (800) 222-3622; in MA, (617) 655-6600.

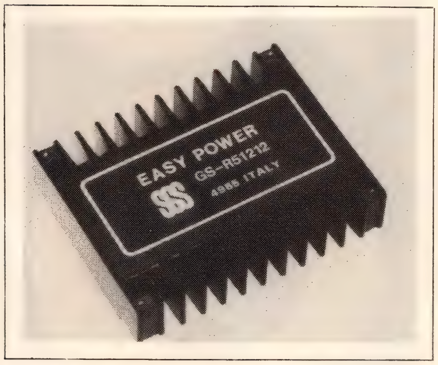
**Circle No 405**

## 80286 EMULATOR

The ICD286 is a 2-board set that plugs into an IBM PC/XT, PC/AT, or compatible and provides full-speed, real-time emulation of the 80286 μP at clock rates as high as 10 MHz. The device features source-level debugging, symbolic single-step, and 2048 bus cycles of real-time trace. It works with executable files under the DOS, PLINK86, and Intel ISIS operating systems. The device supports the IEEE floating-point standard in 32- and 64-bit formats and requires an IBM PC/XT, PC/AT, or a compatible that supports DOS 2.0 and provides at least a 256k-byte memory. The software supports macros and provides a full-screen display with windows for code, data, and machine-state data. The device provides 25 software breakpoints as well as two hardware breakpoints, each with a 16M-byte address range. $5000.

**Answer Software Corp,** 20863 Stevens Creek Blvd, Bldg B-2, Suite C, Cupertino, CA 95014. Phone (408) 253-7515. TLX 296671.

**Circle No 406**

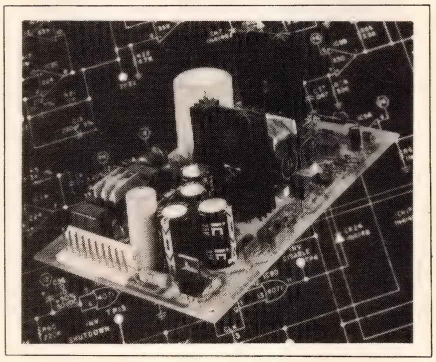



## DC/DC CONVERTER

The GS-R51212 is a 20W dc/dc converter with multiple outputs of 5V at 3.5A, 12V at 0.10A, and −12V at 0.10A. The modules accept input voltages from 10 to 40V dc and are shielded against EMI. The device features a 100-kHz switching frequency that allows high-current operation with 70% efficiency. It measures 8×2.68×3.42 in. and is enclosed in a heat sink with a case-to-ambient rating of 5°C/W of dissipated power. The device also features soft start, thermal and nonlatching short-circuit protection, and reset capability. $65.

**SGS Semiconductor Corp,** 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6245. TLX 249976.

**Circle No 407**



## 50W SWITCHERS

This series of 50W single-output switching power supplies offers a typical efficiency of 70%. Four models are available, with ratings of 5, 12, 15, and 24V. These devices operate from an ac input current of 1.0A rms at 115V ac. They feature built-in EMI filtering, short-circuit protection for all outputs, and overvoltage protection for the 5V output. Hold-up time is 15 msec at full load, while inrush current is 16A at 115V ac (assuming a 15°C ambient cold start). $85.

**Sola,** unit of General Signal Corp, 1717 Busse Rd, Elk Grove Village, IL 60007. Phone (312) 228-1250. TLX 280538.

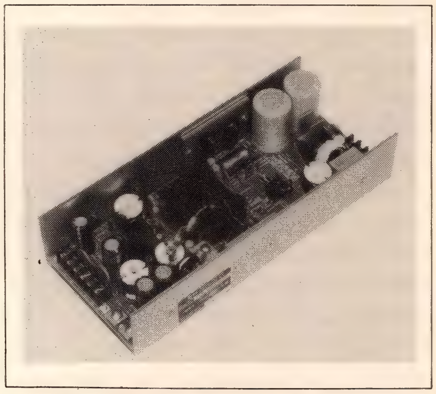
**Circle No 408**

## MAP ANALYZER

The portable Map Tester unit simulates and analyzes manufacturing automation protocol (MAP) networks. The instrument performs automatic simulation and conformance tests of ISO Level III IP (Internet Protocol) and IV TP (Transport Protocol), which parallel the benchmark tests developed by NBS and ITI. Future developments will include simulator support for ISO levels V and VII. The device's operator interface supplies menus and soft keys. The instrument's hardware includes a 68000 μP and two 3½-in. microfloppy-disk drives with 800k bytes of storage. $15,000.

**Tekelec Inc,** 26540 Agoura Rd, Calabasas, CA 91302. Phone (818) 880-5656. TLX 427712.

**Circle No 409**



## 400W SWITCHERS

The MDT-400 Series switching power supplies include models with 50 to 60A with 5V outputs having load and line regulation of ±1%. The 400W multioutput devices measure 1.5×5×2.5 in. and include 12 or 24V, 5% regulated outputs as well as various combinations of auxiliary 5, 12, or 24V floating outputs. The supplies are 75% efficient. The devices comply with UL 478, CSA 22.2, IEC 435, and VDE 0806 safety standards, as well as FCC and VDE (Class A) RFI requirements. $535. Delivery, 30 to 90 days ARO.

**Todd Products Corp,** 50 Emjay Blvd, Brentwood, NY 11717. Phone (516) 231-3366. TWX 510-227-4905.

**Circle No 410**

## REAL-TIME OS

The pSOS-68020 real-time multitasking kernel, the pHILE-68020 file manager, and the pROBE-68020 system debug/analyzer form a family of real-time silicon software components for the company's 68020 32-bit μP. Each component is a plug-in, object-code module independent of target hardware, memory location, or application. The

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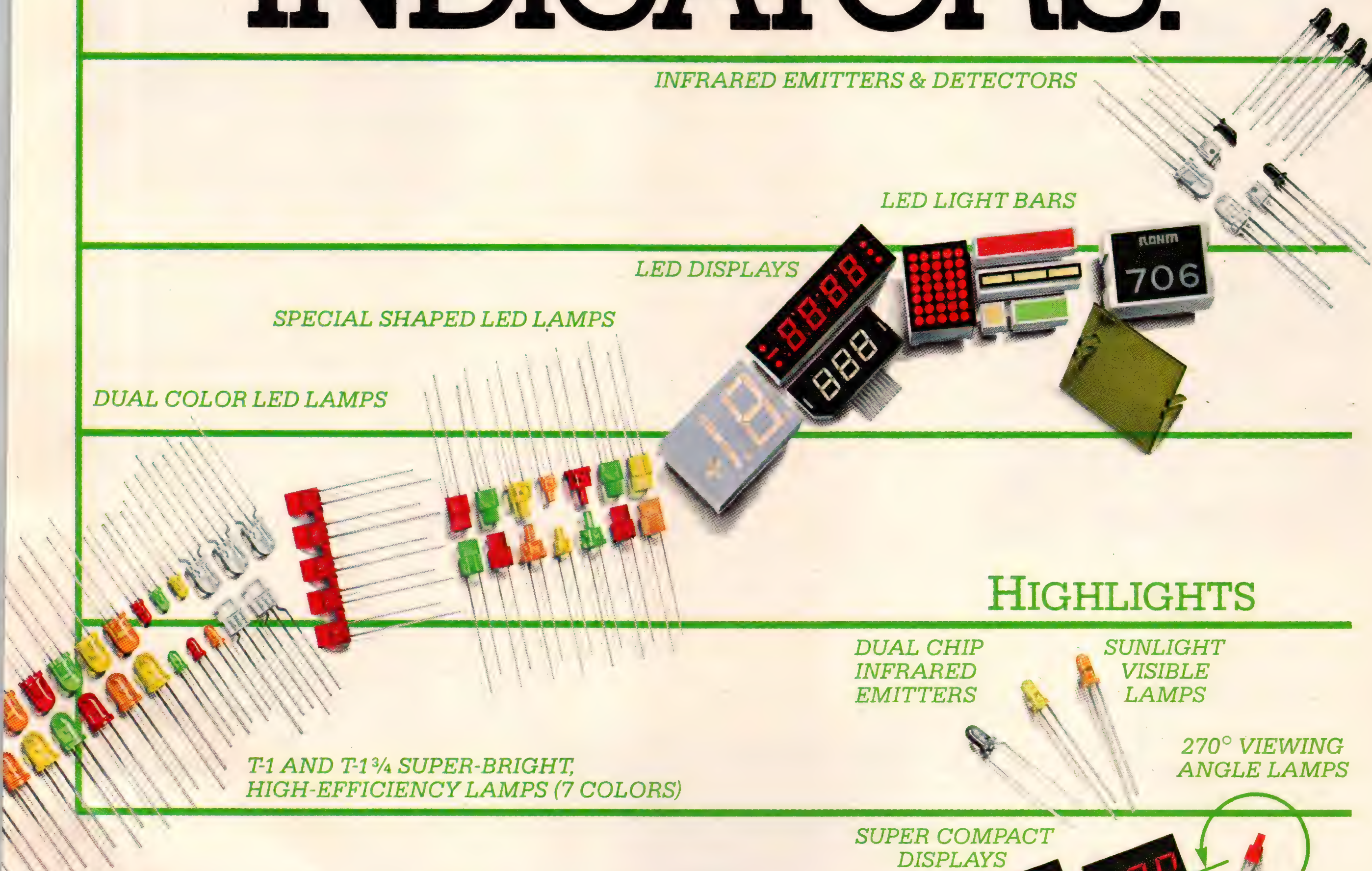


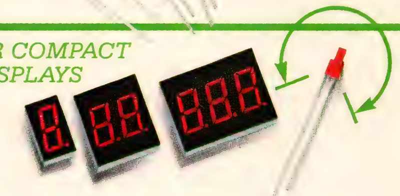


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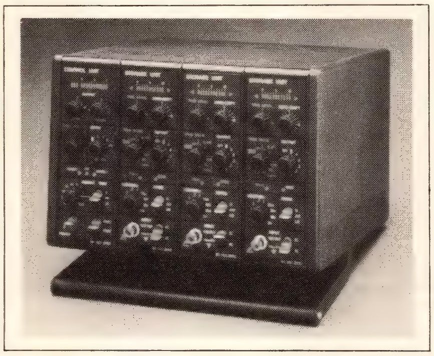
**CIRCLE NO 156**

pSOS-68020 supports dynamic creation and control of processes, message queues, multiple-event synchronization, dynamic allocaton of variable- and fixed-size memory blocks, timing functions, and an I/O supervisor for user-installed drivers. It occupies 5k bytes of code. Its worst-case interrupt response is 15 μsec, and a complex system call with a process switch takes less than 120 μsec. The pHILE-68020 provides contiguous allocation, record locking, and selectable cache write-through features. It fits in 16k bytes of code and operates with any device. The pROBE-68020 is an analysis and integration tool for pSOS-based applications. It provides windows to view processes, queues, and other objects, and breakpoints that trigger on system activities such as state transitions, qualified system calls, and I/O operations. A profiler is included. Package, $9000; each unit, $3000.

**Software Components Group,** 4655 Old Ironsides Dr, Suite 370, Santa Clara, CA 95054. Phone (408) 727-0707. TLX 757697.

**Circle No 411**

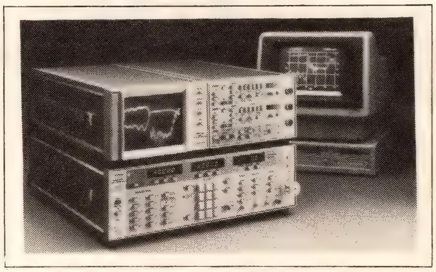


## WAVEFORM RECORDER

The SE 530 3-channel waveform recorder weighs 12 lbs. It handles signals of 250-kHz bandwidth and expands to a system having 30 channels. Each storage module features floating inputs with ranges from 50 mV to 50V and 8-bit resolution. Memory capacity is 16k bytes per channel. You can view stored data with an oscilloscope or transfer it via an RS-232C or IEEE-488 interface. An optional printer, Model SE 531, handles alphanumeric and graphic information. $2840.

**BBC-Metrawatt/Goerz,** 2150 W 6th Ave, Broomfield, CO 80020. Phone (303) 469-5231. TLX 4970869.

**Circle No 412**

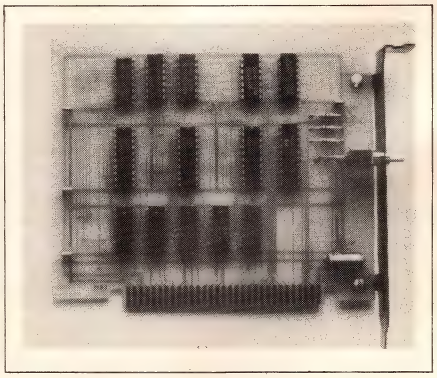


## NETWORK ANALYZER

The model 5672 automated scalar network analyzer system operates in the 40- to 60-GHz range. The 5672 system includes the 560A scalar network analyzer, the 6672A sweep generator, and software. With the addition of waveguide couplers, detectors, and terminations, the software produces hardcopy output within minutes after starting the measurement. $37,885. Delivery, eight weeks ARO.

**Wiltron Co,** 490 Jarvis Dr, Morgan Hill, CA 95037. Phone (408) 778-2000. TLX 285227.

**Circle No 413**



## IBM PC DEBUGGER

The Bug Zapper hardware consists of an IBM PC expansion board containing the Zap circuit and Halt button. The Zap circuit allows you to interrupt your program when a specific memory location is over-

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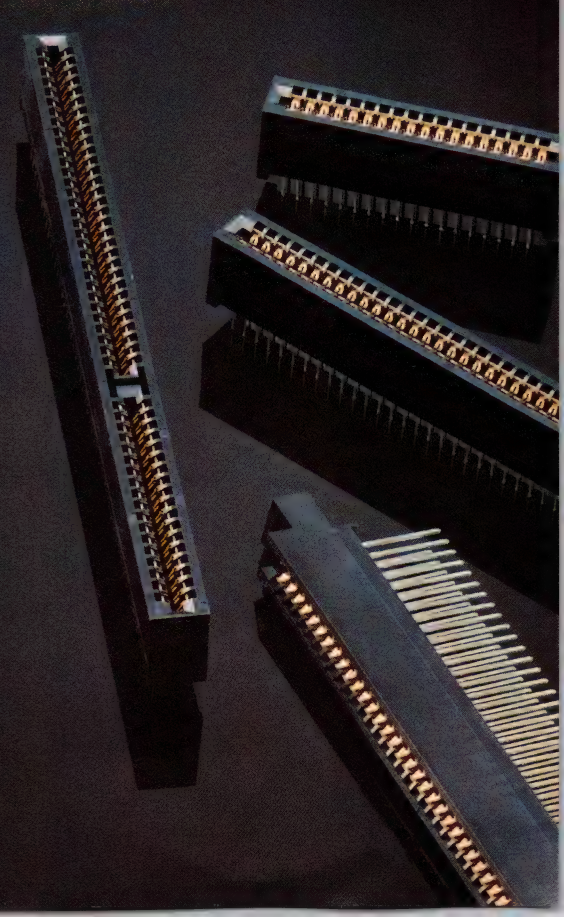
*TWX: 910-494-2094*

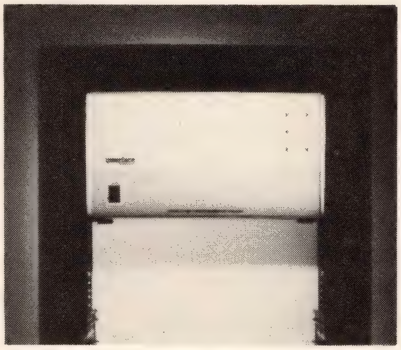

CIRCLE NO 177



written, and the Halt button provides a means to break out of an application and into Guardian. Guardian software loads at boot time and remains dormant while applications execute. The software reactivates via the Halt button or Zap circuit and provides all normal debug commands. The device operates either alone or as a hardware enhancement for your debugger. $195.

**Microtech International,** 9906 Norwood Ct, Dept C-1, Largo, MD 20772. Phone (301) 350-1068.

**Circle No** 414

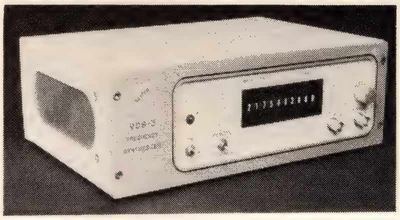


## WORD GENERATOR

System 45 is a Mate-compatible digital word generator optimized for military testing. The device supports all the Atlas digital test types. I/O channels are bidirectional and feature individual 3-state control, mask and compare functions, and 4k-byte memory depth/channel. With a test module adapter (TMA) and a single control chassis containing 64 to 128 bidirectional channels, you can expand your system to contain 1024 channels. The device links with a host computer via an IEEE-488 bus. It achieves throughput rates in excess of 10k bytes/sec and supports the standard Mate-Atlas digital test types defined by USAF specification Mate-STD-2806763 Rev B. $44,000 to $300,000. Delivery, 12 to 16 weeks ARO.

**Interface Technology,** 2100 E Alosta Ave, Glendora, CA 91740. Phone (818) 914-2741.

**Circle No** 415



## SYNTHESIZER

The VDS-3 synthesizer covers DC to 3 MHz in 0.001 Hz steps. Spurious output is $<-55$ dBc, and phase noise is $<-136$ dBc/Hz at a 1 kHz offset. Phase-continuous switching takes place in <500 nsec. You operate the synthesizer in either local mode via thumbwheel switches, or remote mode through a 38-bit TTL-compatible BCD control word. An IEEE-488 interface for remote control is available as an option. A 3-digit BCD word, plus a sign bit, control phase within ±360°, for a total range of 720° in increments of 0.36°. Accuracy is better than 0.1°, and the synthesizer completes controlled phase shift in <0.5 μsec. You can purchase the unit as a completely packaged instrument or as board-level products for OEM use. $1995.

**Sciteq Electronics Inc,** 7380 Clairemont Mesa Blvd, San Diego, CA 92111. Phone (619) 292-0500. TLX 882008.

**Circle No** 416

## LOGIC ANALYZER

The LAS is the first logic analyzer system to make measurements on local-area networks, according to the manufacturer. The device is based on a 16-bit μP mainframe with a CRT display featuring dot graphics, a keyboard, 256k bytes of RAM, a real-time clock, and a 3½-in. floppy disk. The system has options of 20-, 100-, and 400-MHz logic-analysis modules. It also accepts a 48-channel logic generator with a 4000-word memory depth, programmable strobes, macro capability, and a 2-channel waveform analyzer with 20-MHz sampling rate and 8-bit resolution. As many as 96 logic-analyzer channels are available.

The system displays information about real-time interactions in software and hardware systems. $18,480 to $31,590. Delivery, four to 12 weeks ARO.

**Rohde & Schwarz-Polarad Inc,** 5 Delaware Dr, Lake Success, NY 11042. Phone (516) 328-1100. TWX 510-223-0414.

**Circle No 417**

## TWT AMPLIFIER

The A230/A330 series medium power traveling-wave tube (TWT) amplifier features additional capabilities such as RF output-level control, CIIL/MATE compatibility, built-in test features, and programmable leveling. The devices' standard features include mini-tube technology, 10/20W power levels, frequencies to 18 GHz in octave and double-octave bands, push-button operation, digital front-panel display, fault protection, and power-output monitor. The front-panel display indicates collector voltage, helix voltage and current, and RF power output in dBm and watts. $13,700.

**LogiMetrics Inc** 121-03 Dupont St, Plainview, NY 11803. Phone (516) 349-1700.

**Circle No 418**



## LAB SUPPLY

The Model 1630 lab supply provides 0 to 30V at 3A. You can adjust both the voltage and the current output. The supply features built-in metering; two ranges for full- or half-current output, isolated outputs, and reverse-polarity protection. The device has fully adjustable current limiting from 5 to 100% of max output current. It comes with test leads, a spare fuse, a schematic and parts list, and an instruction manual. $225.

**Dynascan Corp,** B&K-Precision, 6460 W Cortland St, Chicago, Il 60635. Phone (312) 889-9087. TLX 253475.

**Circle No 419**

# If your system is only using this many colors,
## isn't it time to grow up?

The INMOS IMSG170 Color Look-up Table offers a grown-up solution to video display color enhancements. It lets you and your RGB analog display advance to a palette of more than a quarter million colors.

This programmable DAC conforms to RS170A standards with pixel rates up to 50 MHz, in a 28 pin package.

And to simplify things, the table integrates the functions of a 256 word x 18 bit color mapping table, three 6-bit DACs, 75 ohm drivers and microprocessor interface into a monolithic CMOS device. The result? Reduced board space and power consumption at a lower cost.

The Color Look-up Table from INMOS. Designing with thousands of colors just became child's play.

INMOS Corporation, Colorado Springs, Colorado, Tel. (303) 630-4000
Bristol, England, Tel. 0272-290-861
Paris, France, Tel. (1) 687-2201
Munich, Germany, Tel. (089) 319-1028

inmos®

Compare your computer design colors to these crayons. If the crayons win, call INMOS.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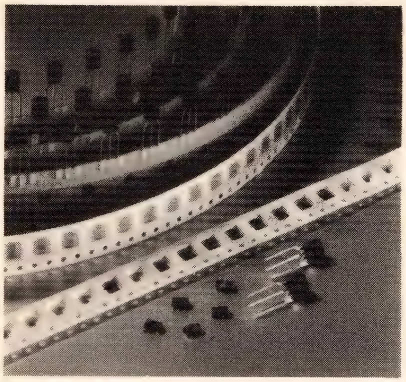
CIRCLE NO 99



## P-CHANNEL FETs

The BST100 and BST110/BS250 feature a low drain-to-source on-resistance (typically 4.5Ω for the BST100 with a gate-source voltage of 10V) and fast switching times (4 nsec turn-on time for the BST110). Low-threshold-voltage values allow you to drive them directly from CMOS or TTL logic. The BST100, the complement of the n-channel BS170A, is rated for a maximum drain-source voltage of −60V, and the BST110/BS250, complement of the BS170, is rated for a maximum drain-source voltage of −50V. The transistors are packaged in TO-92 cases. They are also available as the BST120 and BST122 in SOT-89 packages for surface mounting.

**Philips,** Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

**Circle No 420**

**Amperex Electronic Corp,** George Washington Hwy, Smithfield, RI 02917. Phone (401) 232-0500.

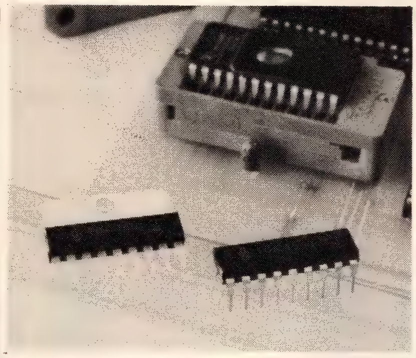
**Circle No 421**

## DISK CONTROLLER

Featuring a hard disk and a DMA controller, this Eurocard HCDC interface board for G64 Bus systems performs high-speed disk access. The disk controller can interface simultaneously to as many as eight disk drives, each with >60M-byte capacity, on which you can implement programmable track formats and data error detection/correction. You can directly connect a variety of drives to the board, including those from Seagate, Epson, NEC, and Rhodime. In addition to providing high-speed data transfer between memory and the hard-disk controller, the 4-channel DMA controller can perform other DMA transfers within the system, including data-chaining functions. BFr 26,000.

**Devlonics Control nv,** Stasegemsesteenweg 110, 8500 Kortrijk, Belgium. Phone (056) 202031. TLX 85643.

**Circle No 422**



## STEPPER-MOTOR DRIVER

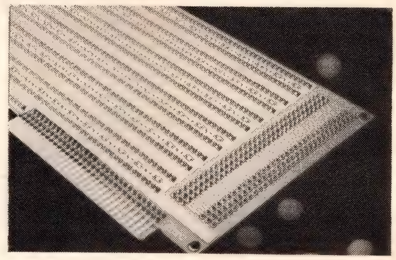
A full-bridge-type driver, the TCA1561 features an output current limit that's voltage programmable to any value ranging to 2A max. Integral flywheel diodes protect the output from inductive overshoot. With the exception of the current-control input, all control inputs are μP compatible. The TCA1561 operates from one supply voltage in the 10 to 38V range and is housed in a 9-pin plastic power SIP that has a cooling tab. The TCA1560, a similar driver, has a 1A max output-current capability and is housed in an 18-pin plastic DIP. TCA1561, DM 9; TCA1560, DM 8 (100).

**Siemens AG,** Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

**Circle No 423**

**Siemens Components Inc,** 186 Wood Ave S, Iselin, NJ 08830. Phone (201) 321-3400.

**Circle No 424**

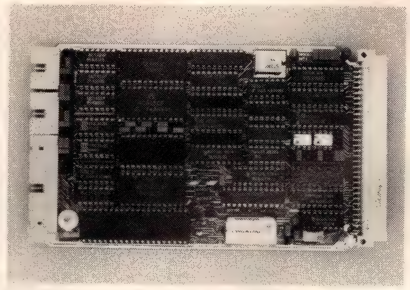


## PROTOTYPING BOARD

For rapid breadboarding of IBM PC-compatible expansion boards, the IQC-PC1 and -PC2 prototyping boards provide you with a standard IBM expansion board footprint and edge connector and a matrix of quick-connect terminal posts. The IQC-PC1 has a provision for mounting a 96-position DIN connector at one end of the board, and the IQC-PC2 has a provision for a 50-position D connector. The quick-connect terminals accept 30 AWG wire, which you can strip off the board after use. Optionally, you can specify the number of populated terminal positions; gold-plated terminals are also available. £165.87.

**Dage (GB) Ltd,** Eurosem Div, Rabans Lane, Aylesbury, Bucks HP19 3RG, UK. Phone (0296) 33200. TLX 83518.

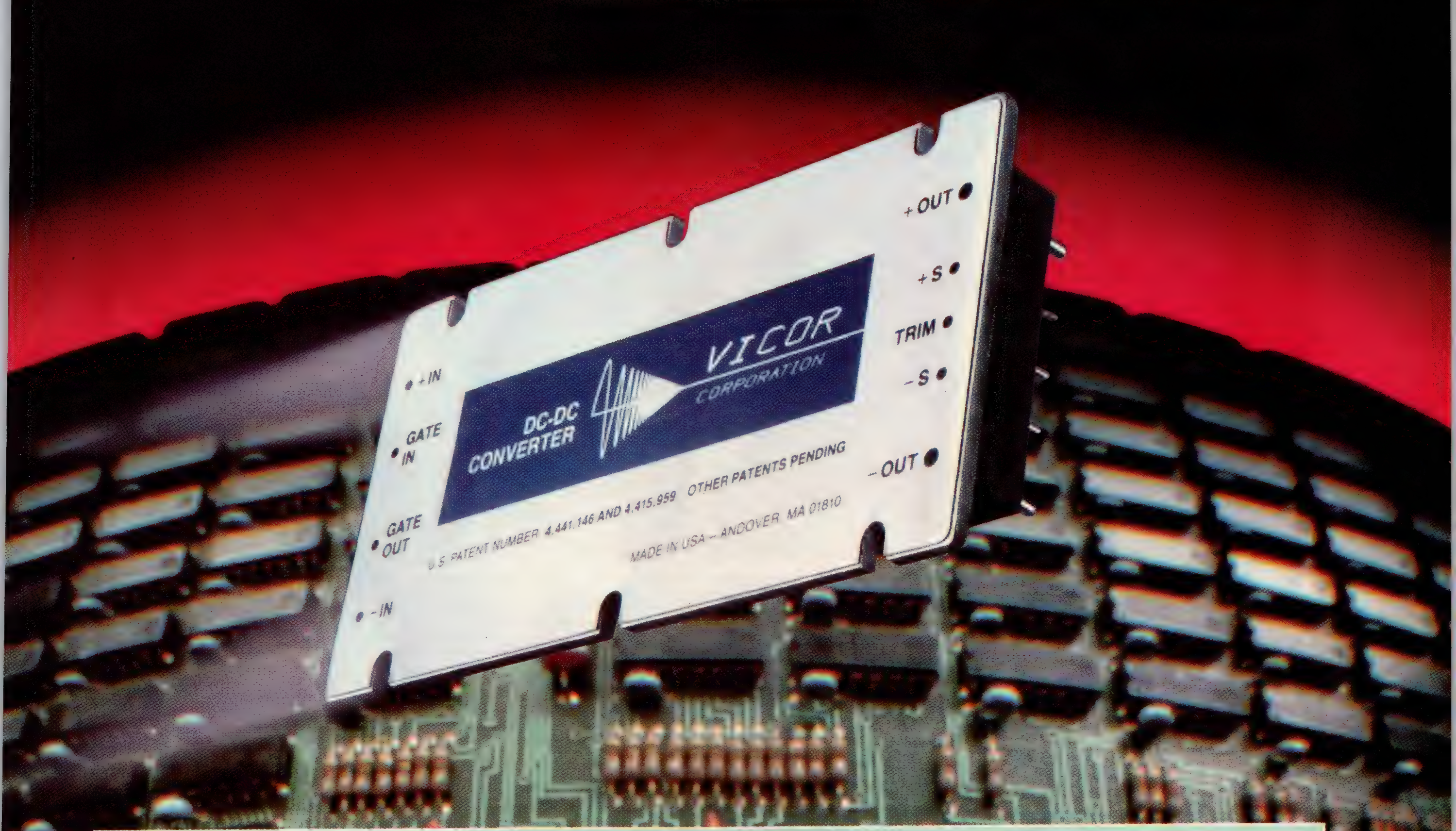
**Circle No 434**



## INTERFACE CARD

The G64/G96-bus compatible GESMFI-1 single Eurocard combines several of the peripheral functions normally required in a computer system. It contains two RS-232C-compatible serial ports, two 8-bit parallel ports, three 16-bit counter/timers, and a battery-backed real-time clock/calendar.

*Power Components Up To 50 Watts/Cubic Inch*




# See Where VICOR's MHz Switchers Can Take You . . .

Vicor's AC/DC and DC/DC converters will take you to the leading edge of power conversion technology. Consider the benefits of our power components in your system:

**SIZE**—A dramatic reduction in converter volume and weight is achieved with MHz switching frequencies. Vicor's VI Series of converters (shown actual size) deliver as much as 200W from a package measuring 2.4″ x 4.6″ x 0.47″ and weighing less than 1/3 of a pound. The converters have power densities as high as 50W/in$^3$, allowing you to design a system that is significantly smaller and lighter than your competitor's using yesterday's power conversion technology.

**EFFICIENCY**—Vicor converters have conversion efficiencies of 80 to 90%. Higher efficiency reduces heat generated in your system making it cooler and more reliable.

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**QUALITY**—Our reputation for quality begins with the design; there are no limited-life components in VI Series converters. Quality is maintained in production with the latest functional testers and burn-in equipment. Each module is tested and trimmed by ATE.

VI-100™ Converters and VIB-00 Power Boosters™, manufactured by Vicor and its licensees, represent the state-of-the-art in power conversion technology. See what smaller size, higher efficiency, and modular component flexibility can do for your next power system design. Call (0734) 868567, TWX: 847073 POWLIN G, FAX: (0734) 755172.

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*VICOR — Component Solutions For Your Power System.*

**CIRCLE NO 172**

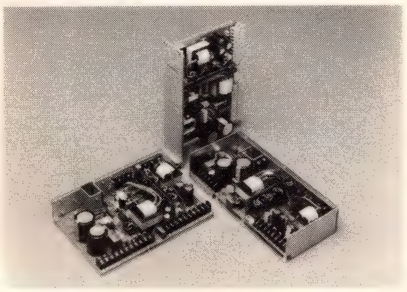
You can independently operate the two serial ports, which have 10-pin connectors, at rates as high as 19.2k baud. The counter/timers are cascadable, and you can program one of the counters to generate an interrupt at intervals of between 30 μsec and 163 sec. The real-time clock calander has programmable alarm and interrupt functions. All onboard devices can generate vectored G64/G96-bus interrupts, and a register stores the board's interrupt status for polled systems. SFr 750.

**Gespac sa,** 3 chemin des Aulx, 1228 Plan-les-Ouates, Geneva, Switzerland. Phone (4122) 713400. TLX 429989.

**Circle No 427**

**Gespac Inc,** 100 W Hoover Ave, Suite 11, Mesa, AZ 85202. Phone (602) 962-5559.

**Circle No 428**



## POWER SUPPLIES

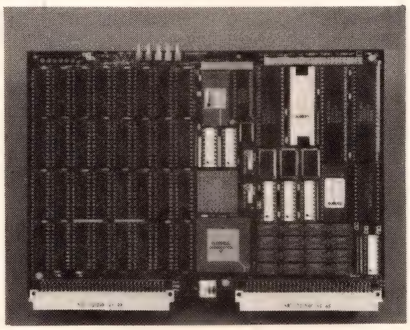
To maintain a small overall size, the Powerite A200 Series of 200W open-frame switching power supplies uses 100-kHz FET switching. The supplies are available in 266×122×57-mm frames and in a standard 159×233×53-mm frames. The latter frame size is available with a 6U×11HP front panel and DIN41612 connectors for Eurorack mounting. You can trade power from the main output of 5V at 40A against the auxiliary outputs of −5V at 5A, 12V at 5A, −12V at 5A, and 24V at 8A, provided the total power output doesn't exceed 200W. Overvoltage and overload protection are standard, and all outputs are protected against short circuits. The supplies, with nominal 110 or 220V ac line inputs, operate over 90 to 132V and 176 to 264V ranges, respectively; soft-start circuitry limits their inrush current to 25A pk. They operate over a 0 to 70°C temperature range but require derating at 2.5%/°C above 50°C. Options include a power-failure alarm-signal module and thermal protection. £170; with front panel and DIN connectors, £190.

**Advance Power Supplies Ltd,** Raynham Rd, Bishop's Stortford, Herts CM23 5PF, UK. Phone (0279) 55155. TLX 81510.

**Circle No 429**

**Advance Power Supplies Inc,** 32111 Aurora Rd, Solon, OH 44139. Phone (216) 349-0755.

**Circle No 430**



## GRAPHICS CARD

Using the power of a 16-MHz 68020 μP as a graphics engine, the Aurora graphics card provides you with onboard firmware for vector, polyline, arc, circle, and area-fill primitives, plus support for high- and low-resolution text fonts and bit-block-transfer raster-manipulation operations. In addition, the firmware includes a complete window-management system with mouse, keyboard, plotter, and terminal-emulation support. The board features 1024×800-pixel resolution, producing a 60-Hz noninterlaced display with configurable monitor and display timings. The 8-bit pixel depth and onboard color look-up table allow you to display 256 colors simultaneously from a palette of 262,144 colors. In addition to the 1M byte of video RAM, the board con-

tains another 1M byte of local RAM for the 68020. Aurora is available on VME Bus, Multibus I, or Multibus II boards, communicating with all these systems via a SCSI Bus interface. You can also control it through one of its four RS-232C serial ports. A 68881 math coprocessor is optional on all versions. As an alternative, you can obtain a manufacturing license. From £3000.

**Tadpole Technology plc,** Cambridge Science Park, Milton Rd, Cambridge CB4 4GG, UK. Phone (0223) 861112. TLX 818152.

**Circle No 431**

## NICKEL SCREENING

Using this spray-on nickel screening compound, you can coat the inside of electronic enclosures with an EMI/RFI shield. The compound provides an even surface coating, which you can apply to a wide variety of materials including ABS and other plastics. The coating is dry after approximately 15 minutes at room temperature. Elevated temperature accelerates the curing process. Typical screen attenuation is 50 dB at 100 MHz. £500 to £600 for 25 liters; £6.50 for 250-gram aerosols (in quantity).

**Electrolube Ltd,** Blakes Rd, Wargrave, Berks RG10 8AW, UK. Phone (073522) 3014. TLX 848797.

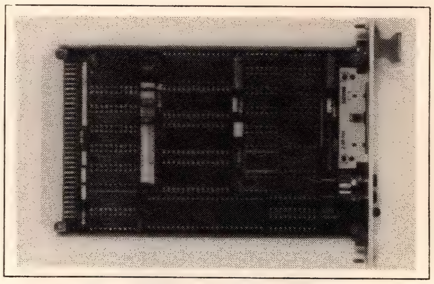
**Circle No 432**

## DEBUGGING SOFTWARE

Using the SEM68000 test/monitor software, you can debug target systems that contain 68000, 68010, or 68020 μPs and perform the debugging either from within a Unix system or via a simple terminal link. The software allows you to download programs developed on the Unix system into the target system, together with symbol tables. The monitor and debugger commands as well as the integral assembler/disassembler recognize these symbols. Monitor commands include run, trace, and breakpoint functions, and its control shell supports macro definitions, so you can, for example, add new commands or execute existing commands. Communication between the Unix and target system via a serial link or via a backplane bus is possible. You can also add driver routines to operate the package from a terminal via a serial link. It is available as source code for Unix System V or as ROMable object code. In ROMable form, the software requires 24k bytes of ROM and 8k bytes of RAM. From DM 5000 in object code form to DM 28,000 as fully documented source code.

**Stollmann GmbH,** Max-Brauer-Allee 81, D-2000 Hamburg 50, West Germany. Phone (040) 3890030.

**Circle No 433**



## SINGLE-BOARD μC

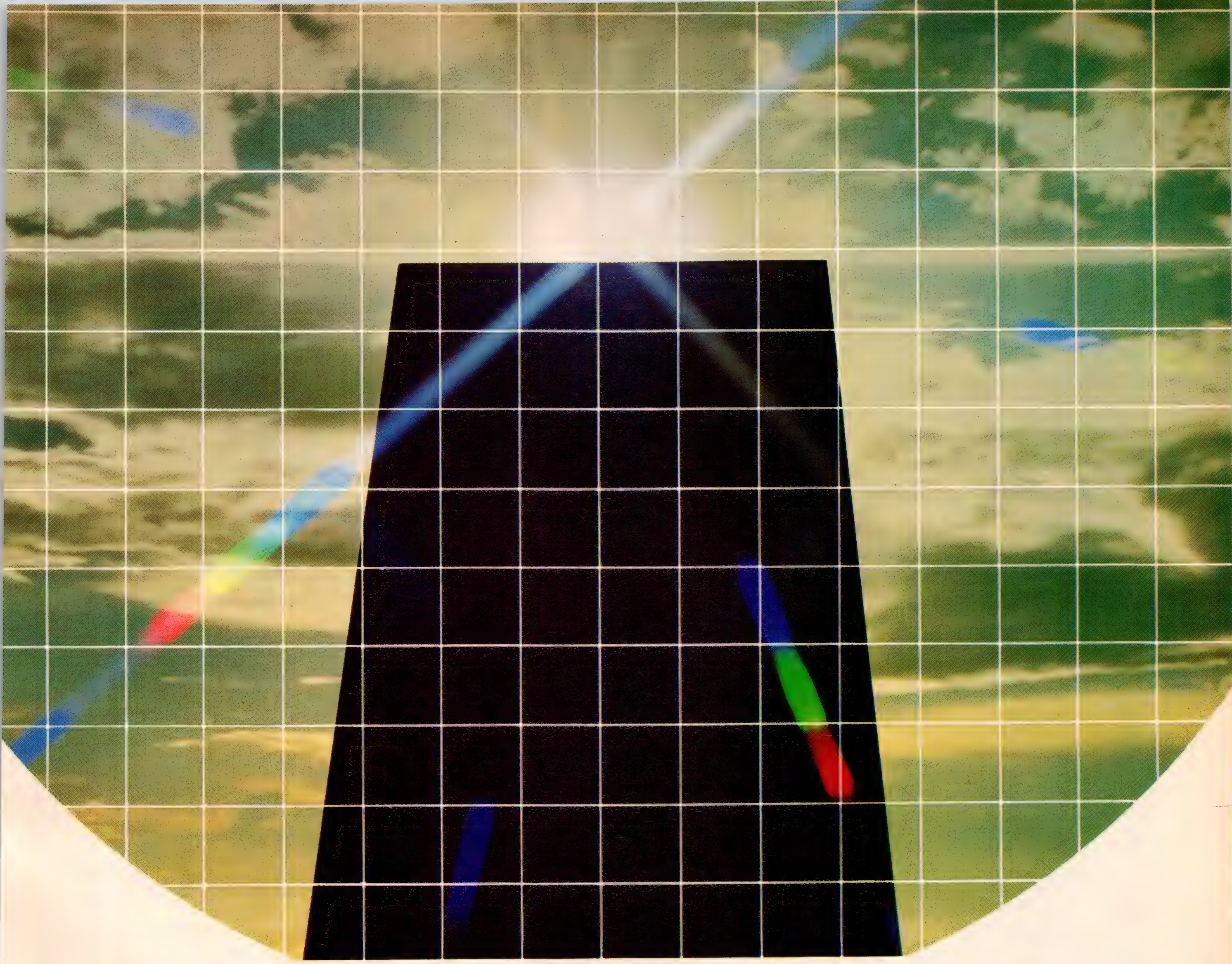
The Eurocard PG8000 computer board is intended for VME Bus or stand-alone operation. It comes equipped with an 8-MHz 68008 μP, two 28-pin byte-wide ROM/RAM sockets, two RS-232C serial ports, a 16-bit timer, and reset and abort pushbuttons. On the VME Bus, the card is suitable for single-processor or multiprocessor applications, and its A24/D8 VME Bus interface includes slot-1 functions, including a single-level bus arbiter. $715.

**Philips,** Industrial & Electro-Acoustic Systems Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757007. TLX 51573.

**Circle No 425**

**Signetics Corp,** 811 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 991-2000.

**Circle No 426**



# ZN454 triple video DAC. It's terrific. It's monolithic!

Ferranti now has a one-chip way to colour graphics. Our new ZN454 combines three video speed DACs in a single 28 pin DIL.

So what do you get? The most cost effective route to colour graphics yet, plus much more reliability.

ZN454 incorporates a separate 4-bit DAC for each of the three colour channels, with composite synchronisation and blanking. So there are 4096 possible display colours.

And with a settling time of 8 nanoseconds and an update rate of 100 MHz the device can interface to monitors with resolution suitable for most computer graphic applications.

Take the monolithic route to colour with Ferranti ZN454. Details from:
IC Marketing, Ferranti Electronics Limited,
Fields New Road, Chadderton, Oldham, OL9 8NP, England.
Telephone: 061 624 0515 Telex: 668038.

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**International Addresses:**
□ Ferranti GmbH, West Germany, Munich, Tel: 089-2368 040 □ Ferranti Electronics Benelux, Antwerp, Tel: (0) 3/542.62.73
□ Ferranti Electronics Sweden, Stockholm, Tel: 08-52 07 20 □ Ferranti Computer Systems (Australia) Pty Limited, Alexandria, Tel: (02) 698 5544
□ Ferranti Wheelock Microelectronics, Aberdeen, Hong Kong, Tel: 5-538298-9 □ Ferranti Electric Inc., USA, New York, Tel: 516-543-0200

CIRCLE NO 43

# ATE at four times the speed of light

## INTERNATIONAL

### MICROPHONE AMP

The ZN482Z buffer amplifier matches a telephone handset's high-impedance electret microphone to the low-input impedance speech amplifier and typically introduces less than 0.06% distortion. Capable of maintaining performance in severe humidity, the buffer loses only 0.4 dB of gain between its input and the negative supply, or 5 dB between its input and the positive supply when the input is subjected to a leakage path as low as 40 MΩ. The buffer is packaged in a TO-92 case and is electrically and mechanically compatible with the PBL3747. £0.40 (1000).

**Ferranti Electronics Ltd,** Fields New Rd, Chadderton, Oldham, Lancs OL9 8NP, UK. Phone 061-624 0515. TLX 668038.

**Circle No 435**

**Ferranti Electric Inc,** 87 Modular Ave, Commack, NY 11725. Phone (516) 543-0200.

**Circle No 436**

### FILTERS

The Series dBZ4/P feedthrough EMI suppression filters have a working voltage of 200V dc and are available with nominal capacitance values of 22 and 44 nF. The filters have a full-spec operating range of −55 to +85°C, but will operate to 125°C if their working voltage is derated to 100V. Manufactured using multilayer discoidal capacitors housed in a metallic tubular body, the filters have a diameter of 4 mm. Their internal construction allows you to assemble the filters using standard 60/40 SnPb solder with a melting point of 180°C. Approximately £2.80 (1000).

**Oxley Developments Co Ltd,** Priory Park, Ulverston, Cumbria LA12 9QG, UK. Phone (0229) 52621. TLX 65141.

**Circle No 437**

**Oxley Inc,** 25 Business Park Dr, Box 814, Branford, CT 06405. Phone (203) 488-1033.

**Circle No 438**

## C COMPILER

The Convex C, a vectorizing C compiler developed for the company's Cray-like C-1 supercomputer, enhances the running of C programs and the use of computing resources. Extensions to the Kernighan and Ritchie specifications include 64-bit arithmetic for engineering and scientific computing, as well as the declaration of data-type enumeration, arrays, structures, and unions of all types. Using the vectorization technique, which exploits the compiler's integrated vector parallelism, the compiler can automatically replace a whole series of machine-language instructions with fewer, more powerful vector instructions. This feature allows the compiler to perform 128 calculations in parallel with a single vector instruction. The compiler also automatically analyzes programs for opportunities to apply vector instructions. $20,000.

**Convex Computer Corp,** 701 N Plano Rd, Richardson, TX 75081. Phone (214) 952-0226.

**Circle No 439**

## GRAPHICS FOR RT

This graphics software product line is now available on the IBM RT PC. As a knowledge-based graphics device management system, GraphCap allows you to use current or new graphics devices on the RT PC without software or hardware conversion. Visual:GKS is a library of subroutines that allow programmers of graphics systems to use a predefined set of graphics capabilities. Visual:C-Chart provides more than 250 functions including routines for axis labeling, automatic scaling, placement of titles and legends, drop shadowing, user-defined markers, and labels. Visual:Pro-Chart is a presentation-quality charting system. Visual:GeniSys comprises a library of 3-D rendering functions for applications in scientific and engineering analysis and simulation, architectural design, mechanical engineering, product design, facilities planning, and animation. All products use GraphCap for device support. Visual:Pro-Chart, $1750; Visual:C-Chart, $1500; Visual:GKS, $695; Visual:GeniSys, $8000 to $12,000.

**Visual Engineering,** 2680 N First St, Suite 200, San Jose, CA 95134. Phone (408) 945-9055.

**Circle No 440**

## MONITORING PROGRAM

XRamp (extended remote-access monitoring program) runs on any MS-DOS μC. Its three major functions are summarizing building-operation data with a daily morning report or other, selectable report formats; archiving files about the history of a building's energy use; and programming the manufacturer's W7000 load control systems from remote locations. It also supports the company's Super Q7000C communications module to monitor Altech solid-state refrigeration pressure control systems. Daily reports comprise one to two pages on energy use, based on data automatically collected during the night. This report correlates kW, kWh, and temperature data collected during the polling routine with similar data for the previous four days. The report also lists and describes any system failures. Optional reports include bypass activity, hourly history, sensor history, thermostat temperatures, contact logging, power reset log, and temperature profiling. You can develop and edit programs for these energy management systems and print them off-line at a remote location. When the program is complete you can download it to the system in two to four minutes. Failure and alarm calls are made automatically to designated phone numbers when an alarm or failure situation occurs. $2300; upgrade from first version, $901.33.

**Honeywell Inc,** Honeywell Plaza, MN12-4162RE75, Minneapolis, MN 55408. Phone (800) 328-5111.

**Circle No 441**

## DATA ACQUISITION

Version 2.7 of Labtech Notebook features RS-232C-device support (universal and menu-driven,) virtual device interface (VDI) graphics support, real-time display options, increased channel capacity, time stamping of data, new serial data-I/O options, and interfaces to more analysis systems. VDI enables the software to use the full resolution of attached devices. This version can work with color-graphics adapters, the IBM enhanced graphics adapter, and the Hercules monochrome board. You can display as many as 50 signals in real time in as many as 15 windows; digital-panel meters and bar charts can display some of the data in analog form. The software supports over 300 data channels, and can write as many as 35 channels to each of 80 disk files. The new serial-I/O options include event counting, frequency measurement, and pulse-train output. Data files can now include the exact time for each data point. $895.

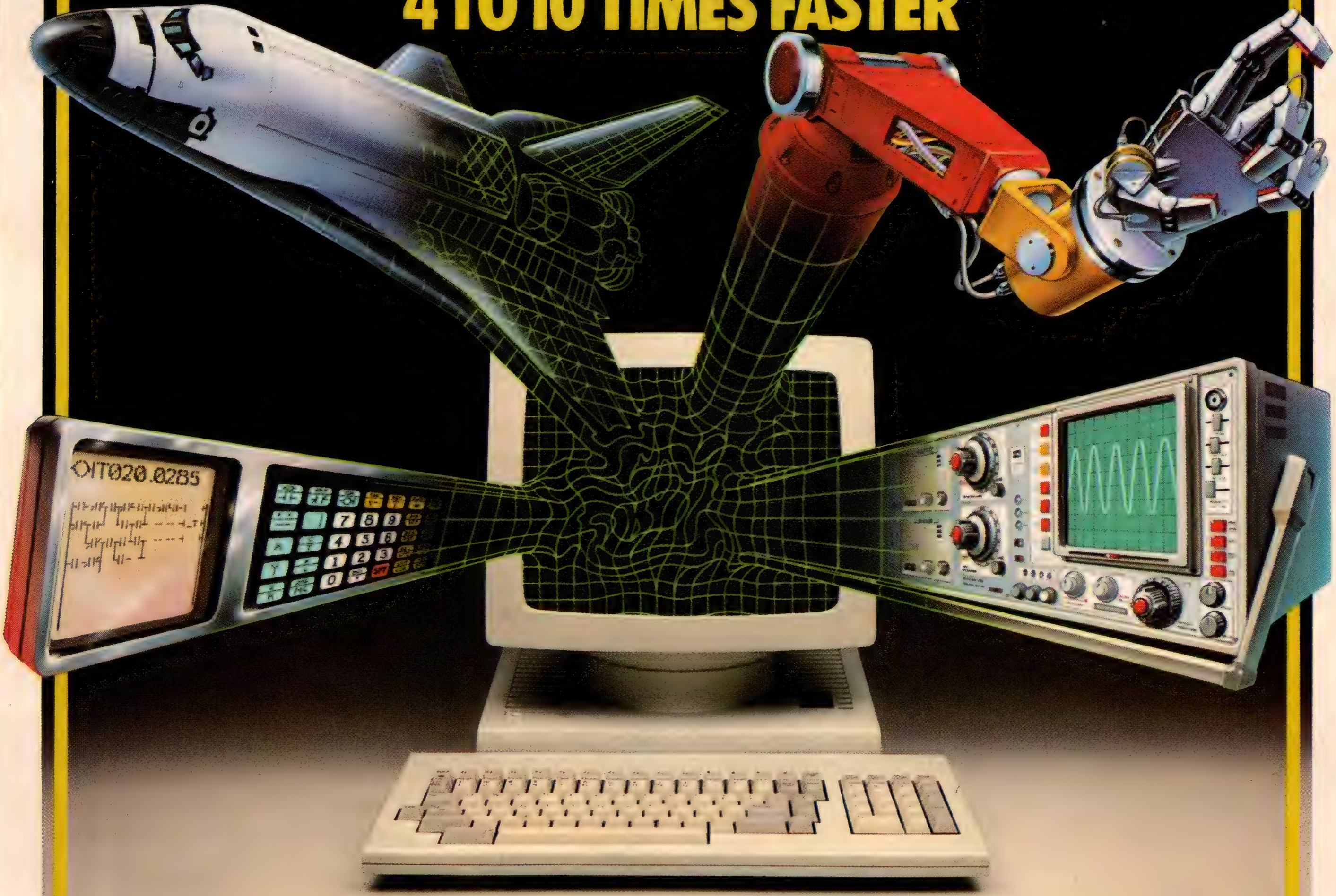
**Laboratory Technologies Corp,** 255 Ballardvale St, Wilmington, MA 01887. Phone (617) 657-5400.

**Circle No 442**

## MULTIUSER DATABASE

A companion product to dBase II Plus, dBase III Plus LAN Pack combines stand-alone and multiuser capability in one package. The software consists of three dBase-access programs, which provide three additional users with economical, net-

# polyFORTH GETS YOUR PROGRAM FROM CONCEPT TO REALITY 4 TO 10 TIMES FASTER



## THE ONLY INTEGRATED SOFTWARE DEVELOPMENT PACKAGE DESIGNED FOR REAL-TIME APPLICATIONS

If you're a real-time software developer, polyFORTH can be your best ally in getting your program up and running on time. In fact, on the average, you will develop a program 4 to 10 times faster than with traditional programming languages.

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polyFORTH shortens development time by making the best use of your time. There are no long waits while you load editors, compilers, assemblers, and other tools, not to mention the long waits while they run—because everything you need is in a single, easy-to-use, 100% resident system. Using polyFORTH, you take a raw idea to fast, compiled code in seconds—and then test it interactively.

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FORTH, Inc.



CIRCLE NO 86

work-only access to dBase III Plus. Each program connects to the dBase administrator (included in the package), which allows multi-user access to data files while preventing simultaneous access to the same record or file. $995.

**Ashton-Tate,** 20101 Hamilton Ave, Torrance, CA 90502. Phone (213) 329-8000. TLX 669984.

**Circle No 443**

## ANALYSIS PACKAGE

Stat68, a statistical package for use with the PDOS operating system on 68000-based systems, is a menu-driven regression-analysis package. The software can tie quality assurance and process monitoring together. This package allows you to edit data and use simple statistics such as mean, standard deviation, variance, maximum, minimum, median, number of data points present, number of missing data points, and correlation between two variables. Once the data is organized, you can plot information as histograms, scatter plots, box plots, residual and partial residual plots, and probability plots. Other statistical features include simple linear, polynomial, and multiple-regression functions; factorial analysis of variance; randomized fixed-block analysis; and latin-squares analysis. $750.

**Eyring Research Institute Inc,** 1450 W 820 St N, Provo, UT 84601. Phone (801) 375-2434.

**Circle No 444**

## FORMAT CONVERSION

Software Bridge converts IBM PC files from one word-processing format to another via a menu-driven program. The program converts between any two of the following systems: Multimate, Displaywrite II and III, Samna Word, Wordstar, Wordperfect, and WordMarc. It also supports DCA (document content architecture) and ASCII file formats. The program runs on any IBM PC, PC/XT, PC/AT, or compatible computer with 128k bytes of RAM. It includes default parameters to resolve inconsistencies between word-processing packages and consequent bad document conversions, such as phantom spaces and rubouts in Wordstar. The program can also resolve other ambiguities by stripping out commands not supported by the receiving word processor. Codes translated by this program include those for hard and soft carriage returns, tabs, underscores, bold face, superscripts, subscripts, merge codes, margins, spacings, and indentations. $249.

**Systems Compatibility Corp,** 1 E Wacker Dr, Chicago, IL 60601. Phone (312) 329-0700.

**Circle No 445**

## PC/RT GRAPHICS

Template, a 3-D graphics software tool, now runs on the IBM PC/RT. Application programs written with this software on other computers can be run on the RT PC. This program supports all available IBM graphics software through the IBM graphics support library; it also provides access to its product-independent device library. The library supports more than 175 different graphics devices. $1000 to $6000.

**Megatek Corp,** Software Div, 9645 Scranton Rd, San Diego, CA 92121. Phone (619) 455-5590. TWX 910-337-1270.

**Circle No 446**

## MATH SOFTWARE

Math/Protran, Stat/Protran, and LP/Protran edition 2.0 are now available for Digital Equipment VAX-11 systems. Using Math/Protran, you can solve mathematical problems in areas such as interpolation and data smoothing, integration and differentiation, differential equations, linear algebraic equations, and random-number generation. Stat/Protran is a problem-solving system for statistics, which can generate statistical analyses in such areas as basic statistics, frequency tables and cross tabulation, correlation, and regression analysis. LP/Protran handles problems in linear programming. Initial annual licenses, $1400 to $2000; renewals, $900 to $1500.

**IMSL,** Sales Div, 2500 CityWest Blvd, Houston, TX 77042. Phone (800) 222-4675; in TX, (713) 782-6060. TLX 791923.

**Circle No 447**

## FORTRAN 77

$F_{77}L$ version 2.0 source-on-line debugger (SOLD) allows you to interface with an executing program at the Fortran level. You can quickly diagnose program errors because SOLD allows you to view your source code, monitor the execution, and examine, modify, and trace the changing values of variables. The ability to handle large arrays is a key feature if you are involved in converting mainframe programs to microcomputers. In version 2.0, the size of commons and arrays is determined by the addressability of the hardware (1M byte). $F_{77}L$ will run on any IBM PC or compatible with MS-DOS, 256k bytes of memory, and a math coprocessor. Version 2.0 is a complete implementation of the ANSI (X3.9-1978) Fortran 77 Standard. $477.

**Lahey Computer Systems Inc,** 31244 Palos Verdes Dr W, Suite 243, Rancho Palos Verdes, CA 90274. Phone (213) 541-1200.

**Circle No 448**

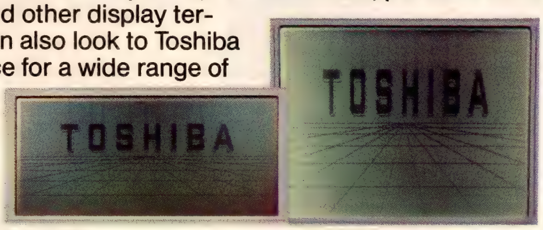

# 2,000 sharper-than-ever characters all on a portable LCD display.

Toshiba's newest LCD modules give you 640 × 200 dot displays in a choice of two viewing sizes. One is approximately the size of a magazine, and the other about half that size.

Both sizes put an enormous amount of information on view . . . an array of 80 characters × 25 lines. But still bulk and power consumption are at a minimum. Battery powered, these slim modules interface with various systems through LCD controller without renewing software.

Toshiba's advanced technology has also eliminated surface reflection and developed a sharper contrast which gives a brighter and easier to read viewing screen. And for low light or dark viewing an optional backlightable LCD is available.

These versatile LCDs are ideally suited for applications as displays for personal computers, POS terminals, portable word processors and other display terminals. You can also look to Toshiba with confidence for a wide range of sizes and display capacity to suit your LCD requirements.




*TLC-363B* *TLC-402*

## Specifications

| | | TLC-402 | TLC-363B |
|---|---|---|---|
| **Display** | | | |
| Number of Characters | | 80×25 (2,000 characters) | 80×25 (2,000 characters) |
| Dot Format | | 8×8, alpha-numeric | 8×8, alpha-numeric |
| Overall Dimensions (W×H×D) | | 274.8×240.6×17.0 mm | 275.0×126.0×15.0 mm |
| **Maximum Ratings** | | | |
| Storage Temperature | | –20° ~ 70° C | –20° ~ 70° C |
| Operating Temperature | | 0° ~ 50° C | 0° ~ 50° C |
| Supply Voltage | VDD | 7 V | 7 V |
| | VDD – VEE | 20 V | 20 V |
| Input Voltage | | 0≤VIN≤VDD | VSS≤VIN≤VDD |
| **Recommended Operating Conditions** | | | |
| Supply Voltage | VDD | 5±0.25V | 5±0.25V |
| | VEE | –11±3V Var. | –11±3V Var. |
| Input Voltage | High | VDD – 0.5V min. | VDD – 0.5V min. |
| | Low | 0.5V max. | 0.5V max. |
| **Typical Characteristics (25°C)** | | | |
| Response Time | Turn ON | 300 ms | 300 ms |
| | Turn OFF | 300 ms | 300 ms |
| Contrast Ratio | | 3 | 3 |
| Viewing Angle | | 15 – 35 degrees | 15 – 35 degrees |

Design and specifications are subject to change without notice.

# TOSHIBA

**Toshiba America, Inc.:** Electronic Components Business Sector: Head Office: 2692 Dow Avenue, Tustin, CA 92680, U.S.A. Tel. (714) 832-6300
Chicago Office: 1101 A Lake Cook Road, Deerfield, IL 60015, U.S.A. Tel. (312) 945-1500
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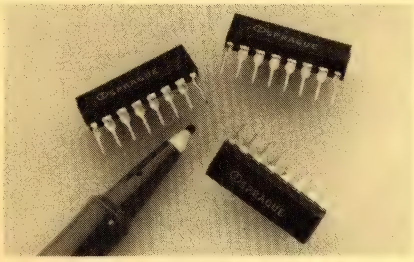
Please circle Reader Service number for additional information from manufacturers.



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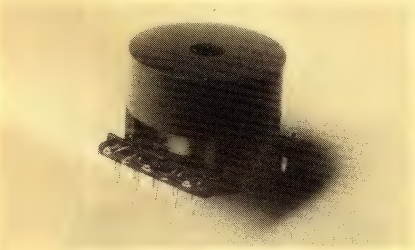

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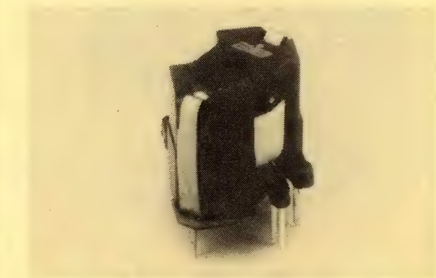

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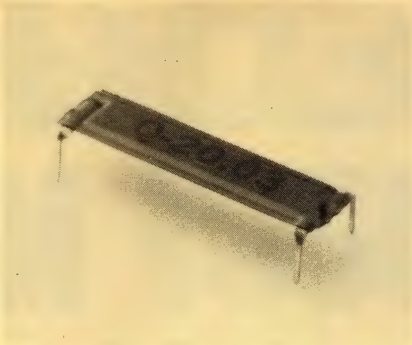

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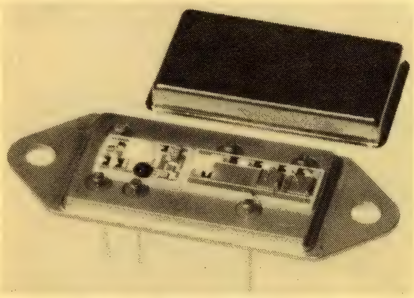

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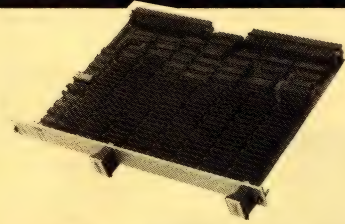

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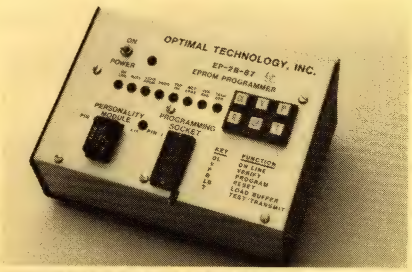

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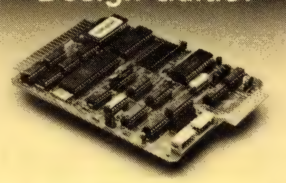

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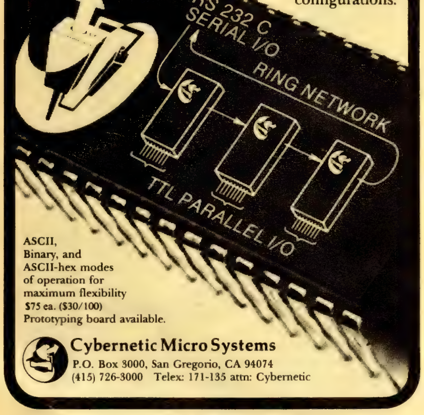


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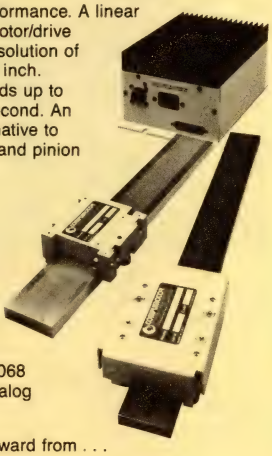

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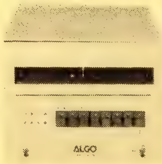

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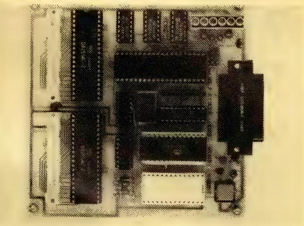

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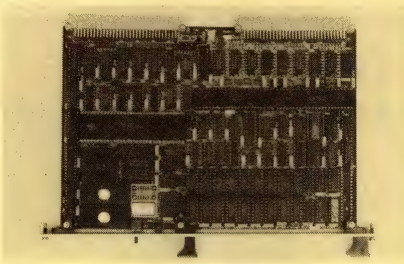

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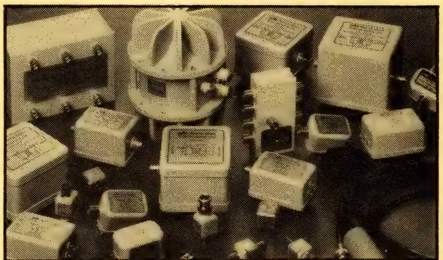

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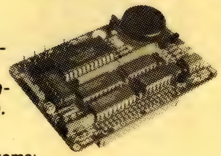

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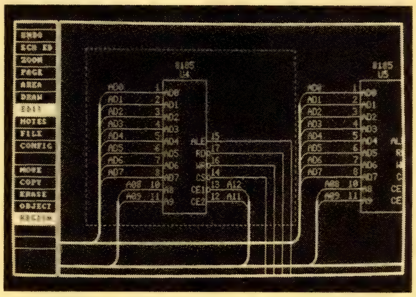

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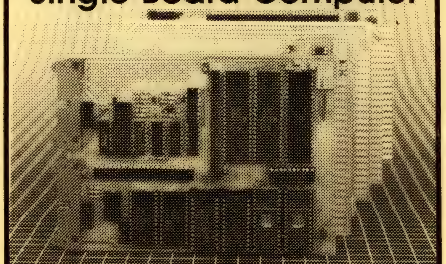
## 6809 Single Board Computer



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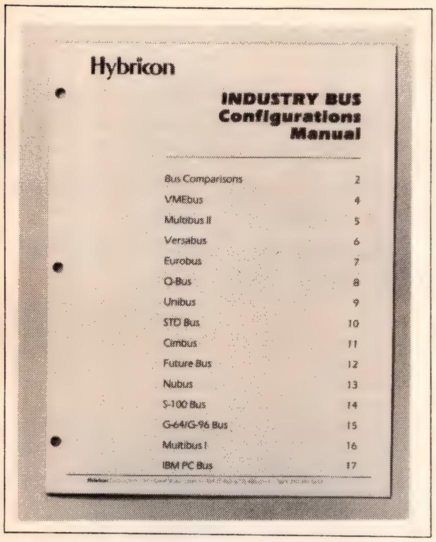


## Manual aids in bus configuration

The *Industry Bus Configurations Manual* provides a reference for 14 widely used data-bus configurations: VME Bus, Multibus I and II, Versabus, Eurobus, Q Bus, STD Bus, Cimbus, Future Bus, Nubus, S-100 Bus, G64/G96 Bus, and the IBM PC bus. The 20-pg book contains such data as characteristics, mechanical specifications, and pinout tables and is 3-hole punched for loose-leaf filing.

**Hybricon Corp,** 410 Great Rd, Littleton, MA 01460.

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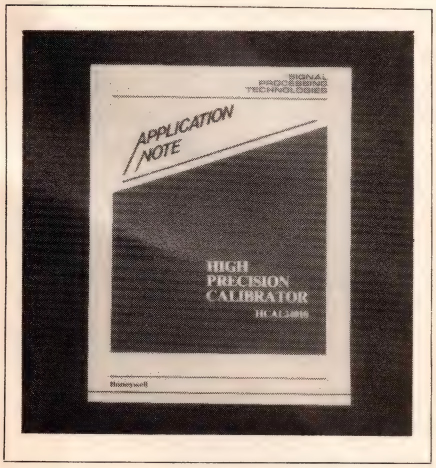


## App note presents data on high-precision calibrator

This 8-pg application note examines the HCAL24010 calibrator, which is designed primarily for front-end calibration, but which can also provide precise programmable scaling of reference voltages. The note depicts the calibrator in the following applications: as a voltage source for calibrating channel gain, as a programmable generator, as an offset-voltage control to the output of an instrumentation amplifier, and as a precision feedback source for a programmable-gain amplifier.

**Honeywell,** Telemarketing Ctr, Box 524, MN12-4164, Minneapolis, MN 55440.

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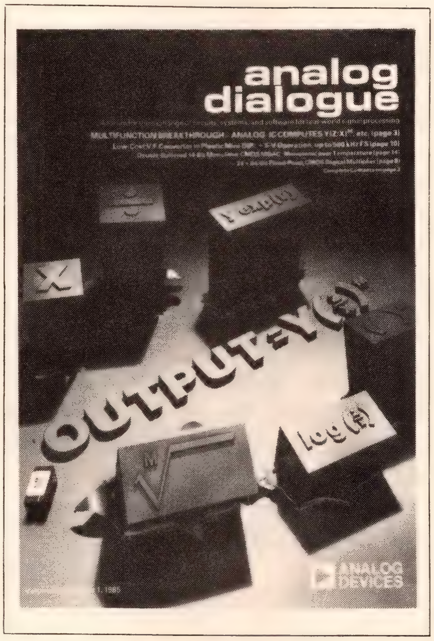


## Journal addresses real-world signal processing

*Analog Dialogue* is a technical journal on circuits, systems, and software for real-world signal processing. This issue describes the AD538, a monolithic, analog computational unit with a transfer function of output=Y (Z/X). Applications illustrate how the chip performs division and multiplication as well as how it computes powers, roots, logs, and antilogs. The publication also contains articles on signal-conditioning modules, converters, and amplifiers.

**Analog Devices,** Literature Ctr, 70 Shawmut Rd, Canton, MA 02021.

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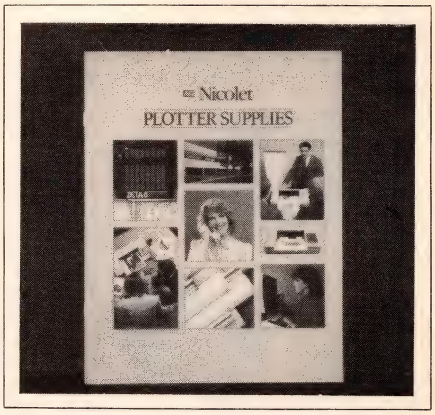



## All about plotter supplies

This 6-pg, 4-color brochure highlights supplies for the vendor's 800 Series of D- and E-size plotters. The booklet features descriptions of available pens—eg, ballpoint, liquid roller, nylon tip, and refillable and disposable liquid ink types—as well as available media—eg, translucent, vellum, bond, and Mylar. Moreover, it contains a chart to help you select the optimum combination for your application, including recommendations and ratings for each combination. The brochure also lists other accessories.

**Nicolet Computer Graphics,** 777 Arnold Dr, Martinez, CA 94553.

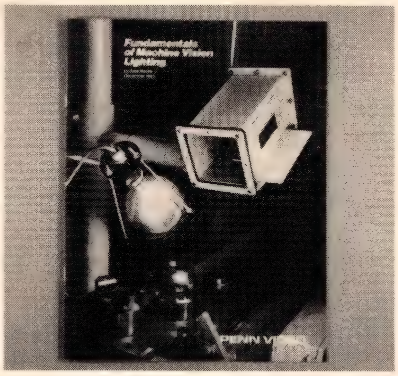
**Circle No 452**

## Brochure introduces CAMAC specifications

This 16-pg pamphlet is intended to familiarize the reader with CAMAC, the IEEE-583 international standard for computer automated measurement and control. Suitable as an introduction to the standard's basic specifications, the brochure describes the functions of a CAMAC module, crate, and crate controller. It also covers serial- and parallel-highway modes of data transmission, distributed intelligence, and the in-crate Dataway communication flow between process modules and crate controller. Charts and diagrams complement the text.

**KineticSystems Corp,** 11 Maryknoll Dr, Lockport, IL 60441.

**Circle No 453**




## Document explores machine-vision lighting

*Fundamentals of Machine Vision Lighting* is a 12-pg publication that presents techniques for solving machine-vision lighting problems, including applications examples. It considers the factors you must take into account when addressing an application and describes three approaches: front lighting, backlighting, and structured lighting. In addition, it discusses several illumination sources, including incandescent bulbs, fluorescent and Xenon tubes, lasers, and infrared LEDs. Twenty-eight figures and photos supplement the text.

**Penn Video,** 929 Sweitzer Ave, Akron, OH 44311.

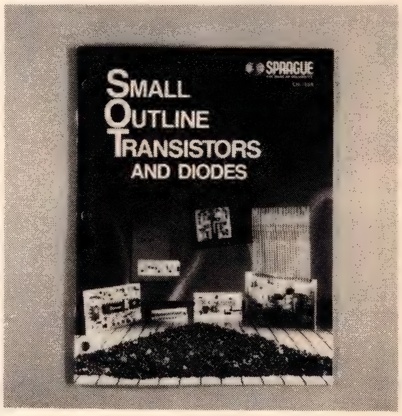
**Circle No 454**

## Catalog offers selection of handbooks

This 15-pg pamphlet is a compilation of the handbooks, services, and reports that this company offers. Each entry includes a description and overview of each particular offering. Examples of available handbooks include *The Handbook on Marketing for High-Technologies' Top Managements*, *The Marketing Book of Numbers*, and *The Revised Handbook on Distribution. Mainly Marketing* is a monthly report that alternates industry-marketing survey findings with tutorial articles on high-tech marketing. *Forecasting Electronic Business,* a special issue of the monthly report, describes how you can use publication data to your best advantage. The pamphlet also covers marketing-consultant and seminar services. The booklet is free, but by sending a \$0.56 stamped, self-addressed 6×9 envelope, you can obtain a sample copy of *Mainly Marketing.*

**Schoonmaker Associates,** Drawer M, Coram, NY 11727.

**Circle No 455**




## Brochure expands on semiconductors

This newly revised brochure presents the manufacturer's semiconductors housed in 3-pin SOT (small-outline-transistor) packages. Among the products covered are npn and pnp bipolar transistors, junction FETs, Schottky diodes, zener diodes, single and dual diodes, and series diodes. The booklet offers electrical characteristics, pinouts, reliability data, and package dimensions for the various semiconductors. The 24-pg brochure is 3-hole punched for loose-leaf filing.

**Sprague Electric Co,** Box 9102, Mansfield, MA 02048.

**Circle No 456**

## Data book references small-signal FETs

This 343-pg manual provides specs and performance data for more than 350 of the company's FET products. The book updates an earlier publication. For example, it contains 41 new industrial and military FETs,

including the DMOS line: n-channel enhancement- and depletion-mode devices that offer ultrahigh-speed switching. A 107-pg applications section offers tips, including how to use the FETs as oscillators, switch arrays, and mixers. Eight new application notes feature the FETs as amplifiers, current protectors, current sources, and analog switches. An added design-alternative section illustrates approaches that use FETs to enhance circuit performance. In addition, the compendium provides die-process, topography, and package information; a 20-pg selector guide; and a small-signal FET cross-reference. $12.

**Siliconix Inc,** 2201 Laurelwood Rd, Santa Clara, CA 95054.

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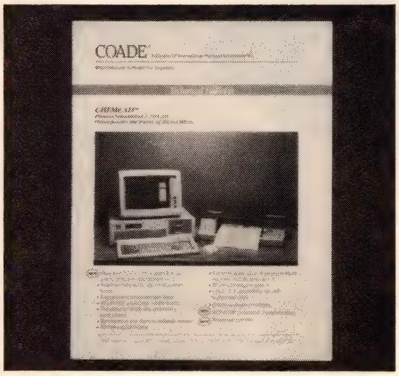
## App note for telecommunications design

Containing 24 pages, this application note presents various implementations for the G65SC150 communications terminal unit, including DTMF dialing, dial-pulse signaling, 0- to 600-baud modems, UARTs, and keyboard scan. The note features a 300-baud modem application and provides detailed programs and diagrams that illustrate the unit's telecommunications-design capability. It also offers design suggestions for using the G65SC150 as a clock oscillator and as a reset circuit, as well as for external memory operation, bus expansion, and operation in special low-power modes. It provides a functional system (the G65DS-150 evaluation board) that you can fabricate to evaluate the programs offered.

**GTE Microcircuits,** Marketing Services, 2000 W 14th St, Tempe, AZ 85281.

**Circle No 458**




## Bulletin portrays 2-D CAD

This 6-pg, 4-color technical bulletin characterizes Chemcad, a 2-D CAD system for process flow diagrams, graphics, and spreadsheets. The brochure summarizes the software's capabilities and lists its built-in simulation functions. Other topics covered include hardware requirements, thermodynamic and input options, and the components library. The pamphlet also depicts examples of the output available from the system—eg, tray profile, output flowsheet, and equipment-design data.

**Coade,** Div of International Thomson Information Inc, 8550 Katy Freeway, Suite 122, Houston, TX 77024.

**Circle No 459**

## Learn about grounding requirements

"Computer Grounding," an 8-pg paper, discusses the special electrical grounding that magnetically sensitive computers demand, as well as provisions of the National Electrical Code (NEC). The paper covers such subjects as fault current protection, hazardous touch potential, voltage reference at RF frequencies, shield grounding, and NEC requirements. In addition, diagrams and photos show details of a complete computer-grounding system and a resulting signal reference grid.

**Erico Products Inc,** Erico Rd, Solon, OH 44139.

**Circle No 460**

## Pamphlet provides data on modem

This pamphlet portrays Race (remote asynchronous computer extension) modems, including detailed data on tower (vertical) and traditional (horizontal) models. The 8-pg, 4-color brochure provides background information on data communications and describes how these modems circumvent the problems normally associated with such communications. In addition, it devotes one page to a diagram of the modems' operating-control panels, including explanations.

**Data Race Inc**, 5839 Sebastian, San Antonio, TX 78249.

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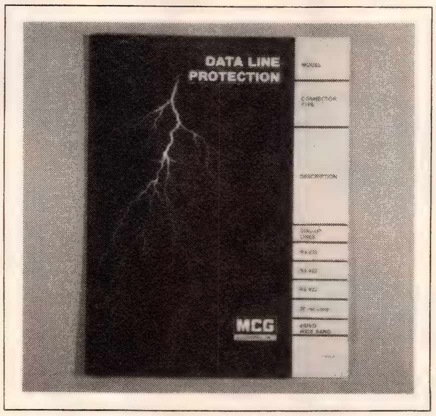


## Catalogs cover data-, power-line protection

These two catalogs present information on the manufacturer's data-line protectors and ac-power-line protectors, respectively. Each brochure contains technical specs, installation data, mounting diagrams, and an application guide. The ac-power-line catalog covers six protectors, including plug-in protectors and heavy-duty facility protectors. Each catalog contains separate price-list inserts.

**MCG Electronics Inc,** 12 Burt Dr, Deer Park, NY 11729.

**Circle No** 462

## Brochure highlights pen plotter

This brochure details the MP 2000, a B-size, flatbed 8-pen plotter. The 4-color document covers all interface specifications and describes the HP/GL and GP/GL protocol commands. It also depicts examples of various application programs.

**Western Graphtec Inc,** 12 Chrysler St, Irvine, CA 92718.

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# BUSINESS/CORPORATE STAFF

**F Warren Dickson**
Vice President/Publisher
Newton, MA 02158
(617) 964-3030
Telex 940573
Diann Siegel, Assistant

**Peter D Coley**
Associate Publisher/
Advertising Sales Director
Newton, MA 02158
(617) 964-3030
Stacey Vorias, Assistant

**NEW ENGLAND**
Bob Sommer, Regional Manager
275 Washington St
Newton, MA 02158
(617) 964-3030

**STAMFORD 06904**
George Isbell, Regional Manager
8 Stamford Forum, Box 10277
(203) 328-2580

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Daniel J Rowland, Regional Manager
Chris Platt, Regional Manager
475 Park Avenue South
(212) 576-8014
(212) 576-8017

**PHILADELPHIA AREA**
Steve Farkas, Regional Manager
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(215) 293-1212

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**AUSTRIA**
Igal Elan
Elan Marketing Group
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**SOUTHERN EUROPE**
Igal Elan
Elan Marketing Group
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**FAR EAST**
Ed Schrader, Director of Sales
18818 Teller Ave, Suite 170
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Dynaco International Inc
7-2-8 Minamiaoyama
Minato-Ku,
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Tel: 011-81-3-409-4569
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**TAIWAN**
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Box 26-578
Taipei, Taiwan
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**PRODUCT MART**
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475 Park Avenue South
New York, NY 10016
(212) 576-8049

Dan Brink
Western Sales Manager
2041 Business Center Dr, Suite 109
Irvine, CA 92715
(714) 851-9422

Maria Cubas
Production Assistant
(212) 576-8045

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| Memory Depth | 2K | 1K | 4K |
| State/Timing Correlation/ Display | No | No | Yes |
| **Timing Logic Analysis** | Yes | Yes | Yes |
| Acquisition Speed | 100MHz | 100MHz | 100MHz |
| Channels | 18 | 8 | 16 |
| Transitional Timing | No | No | Yes |
| **Pattern Generation** | No | No | Yes |
| Channels | – | – | 160 |
| Speed | – | – | 20MHz |
| Vector Depth | – | – | 8K |
| **Software Analysis** | assembly only | assembly only | high-level and assembly |
| Symbolic Trace | No | No | Yes |
| Performance Analysis | statistical | statistical | real-time non-statistical |
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# Women in engineering serve as role models to fight image of male-dominated profession

Deborah Asbrand, *Staff Editor*

During the 1970s, the engineering community appeared to be on the path to becoming a more diverse body of professionals. Ripple effects from the women's movement and the civil rights activities of the 1960s created a climate of new opportunity for women and minorities. Professions that traditionally had been closed off to them suddenly opened their doors.

The atmosphere of encouragement worked: Enrollments of black and Hispanic freshmen in electrical engineering programs nearly doubled between 1971 and 1982, rising from 5.4% of all enrollments to more than 10%. Women were attracted to the programs in even greater numbers. Female freshmen enrollments in electrical engineering programs jumped from a scant 2.6% in 1971 to 17% in 1982.

Yet since 1982, minority enrollments have leveled off, and women's enrollments have dropped back both in absolute numbers and as a percentage of all enrolled students. The sociological and economic factors that combine to produce fewer women and minorities in engineering are complex; career opportunities are showing improvement in some areas, while in others, stereotypes and roadblocks to management-level positions remain. But the reasons for the slowdown in college enrollments are much simpler. For women, these reasons are a decreased emphasis on affirmative action and the lingering stereotype of engineering as a man's profession. This article, the first of a 2-part series, looks at the engineering environment women find themselves in today.

"The heat is off" with regard to affirmative-action programs, says Shirley Malcolm, director of the American Association for the Advancement of Science's Office of Opportunities in Science. With affirmative action no longer a politically popular cause and conservative values now in vogue, Malcolm says, the promotion of equal opportunities has become a low priority on the agendas of both the private and public sectors. Although this climate does not deter women who have already decided upon engineering as a career, it exerts its influence on young women who are poised to make a career choice.

*Women in engineering say what's striking about them and their male counterparts are their similarities, not their differences. Yet some find that, in certain quarters, standards and attitudes of a bygone era continue to exist.*

Some worry that the flush of success sustained by 1970s efforts to encourage women into engineering could fade if academia and industry slacken their emphasis on those efforts. "The real danger is people thinking we've got the problem licked," says William LeBold, director of Purdue University's Education Research and Information Systems. "The fact is engineering still has the lowest level of women in any occupation except the military." Indeed, while 20% of all chemists and 29% of all computer specialists are women, only 5.7% of engineers are women.

Contributing to women's small numbers in engineering is the firmly entrenched belief that science-related professions are for men only. Such widely held beliefs are fed by, and in turn reinforce, powerful social influences, says Malcolm, who also is the outgoing chairman of the National Science Foundation's Committee on Equal Opportunities in Science and Technology. "If your son doesn't do well in math, you get him a tutor. If your daughter doesn't do well in math, she doesn't need it," says Malcolm, reciting a commonplace bias in our culture.

Women who are already working as engineers don't believe that statistics that show them to be a small minority within their profession should intimidate anyone. What's striking about these women and their male counterparts, they say, are their similarities, not their differences. Women choose careers in engineering for the same reasons men do: They enjoy math and science in school and are intrigued by engineering's hands-on work. "I liked the hands-on aspect," says Annette Gathright, a staff engineer at Interstate Electronics Corp in Anaheim, CA. "I've always worked with my hands and my head. I'm a creative person under all this scientific training. And a natural extension of that for me was engineering."

In addition to an interest in math and science, the common denominator among women who choose an engineering career is that, like their male counterparts, they were never told that they couldn't, or shouldn't, pursue their technical interests.

*Thelma Estrin, engineering professor and assistant dean: "There is still the perception that it's harder for a woman to go up the ladder, primarily because there aren't any role models at the top."*

When members of the Boy Scout troop that Gathright's father led built crystal radios, Gathright was encouraged to join in and build her own.

"I grew up in an environment where it was never a question of 'can I do it,'" says Judy Estrin, executive vice president for research and development at, and one of the four founders of, Bridge Communications, a Mountain View, CA, manufacturer of LAN products. "I never thought about whether I could do it; I just assumed I could."

**Following your own interests**

"It just never occurred to me that I couldn't do anything I wanted to do," echoes Mary Rogers, a senior systems test engineer at Lockheed Missiles and Space Co in Sunnyvale, CA. Born and raised in Brazil, Rogers attended an American school there and then completed her last three years of high school by correspondence. Away from the social conventions that existed in the United States during the 1940s, Rogers felt free to choose the career that most interested her.

In most cases, each of these women found that she was one of just a few female students who pursued advanced science and math during high school. Each was thus unperturbed by the even smaller numbers of women in college science and engineering classes. Rogers says her presence as a woman went largely unnoticed by her male engineering classmates. And although Gathright didn't meet another female engineering student until her junior year, her interest in her studies superseded any differences between her and her male classmates. "In my junior year, the more I got into electives that involved electronics, the more enthusiastic I got and the more I enjoyed it. It fascinated me."

Wanda Garrett, an applications engineer for National Semiconductor in Santa Clara, CA, was one of four women among the 60 students studying electrical engineering in her class at Washington State University in the early 1980s. The four women became close friends and roommates. "I think the thing we all agreed on was that no one had told us we couldn't [choose engineering] or could give us any reasons why we should not," Garrett says.

For some of these women, the first instances of resistance to their career choice occurred once they left college and began looking for a job. When Gathright began meeting with on-campus recruiters during her senior year at Arizona State University in 1969, "some representatives flat out said 'you're a woman, and we're not going to make you an offer,'" she recalls. Others asked questions about what she would do with her children while she worked (she had two children at the time), how many children she planned to have, and what her husband did for a living. Other companies, however, were supportive. During a company visit to General Electric's Informations Systems facility in Phoenix, AZ, Gathright was given the opportunity to talk with a woman engineer who had already spent several years with the company.

Years later, some women continue to face the problems Gathright encountered. When one of Garrett's roommates accepted a job offer from a company with which she had interviewed, the company's representative responded by saying, "Good, now we've met our quota."

In spite of these lingering attitudes, more and more doors are opening. For one thing, the great demand for talented engineers has led to a much improved scenario for recent female engineering graduates. Barbara Mulkey, a 1982 graduate of Purdue University's honors program in engineering, found her skills in healthy demand. She interviewed with 30 companies during

her senior year and made seven company visits. After accepting a job with General Electric, she was one of 150 new engineers selected to participate in the company's Edison Engineering Program, a prestigious, 2-year training program that includes part-time graduate study. She now works as a systems-analysis engineer at the Military and Data Systems Operations of GE's Space Systems Division in Valley Forge, PA.

Many young women in engineering report that the doors of opportunity are opened as widely for them as for their male counterparts. Their college and industry experiences have been free of any gender-related problems, and they see their own careers paralleling those of their male colleagues. "Although people like to talk about the issue of women in engineering, there isn't much of an issue," Mulkey finds. Estrin believes that the shared technical knowledge on which the engineering profession is based is making possible the engineering population's transition to a more diversified group. In engineering, she says, "you have a basis on which to prove yourself. You can establish credibility relatively quickly by discussing technical aspects."

Yet the image of engineering as a male profession dies hard. One of a team of analog applications engineers, several of whom are women, Wanda Garrett frequently speaks with customers over the telephone. "We get calls from customers who think we're secretaries," she says. "They almost refuse to believe that we understand the technology. It's almost comical sometimes when we try to convince them that we can help them with their technical problems."

*Annette Gathright, staff engineer: "I've always worked with my hands and my head. I'm a creative person under all of this scientific training. A natural extension of that for me was engineering."*

**$11,000 salary gap**

Stereotypes like these continue to dog students' career choices. A recent report by the Congressional Office of Technology Assessment found that stereotyped career expectations are a major obstacle preventing more women from entering engineering. But along with their perception that engineering is a profession for men, many women sense that working in a male-dominated work force will hinder their professional success materially. Some sobering facts support their perceptions: A 1982 survey of IEEE members found that the average male member earns $11,700 more than the average female member. Taking into account the fact that men have more experience, which drives up their average salary, the study still concluded that the average IEEE man earns $2600 more than the average IEEE woman.

The National Engineering Career Development Study, directed by Purdue's LeBold, augments these findings. It found that, although men's and women's entry salaries are comparable, a pay gap opens early in their careers that increases with years of experience. Significantly, the study also found women much less likely to be chosen for management positions. "By and large there is still the perception that it's harder for a woman to go up the ladder, primarily because there aren't any role models at the top," says Thelma Estrin, mother of Judy Estrin and a professor and assistant dean in the school of engineering at the University of California at Los Angeles. "People just aren't used to seeing women in those positions."

The elder Estrin has direct experience with such roadblocks. She earned undergraduate, master's, and doctoral degrees in electrical engineering at the University of Wisconsin, from which she graduated in 1951. Her first job was at Columbia Presbyterian Hospital in New York City, where she worked analyzing brain waves, but the dim prospects of parlaying her exceptional talents into a fulfilling career

in industry forced her to turn toward academia.

In 1960, Estrin joined the Brain Research Institute at UCLA's Health and Science Center as director of its data-processing laboratory. There she set up electronics and computer facilities for measuring, recording, and analyzing the activity of the brain. Since then, in addition to becoming a professor and an assistant dean at UCLA's school of engineering, she has directed the division of electrical, computer, and systems engineering within the National Science Foundation's engineering directorate and has served as a member of the IEEE's board of directors and as its executive vice president. She was also the first woman to serve on the Aerospace Board of Trustees, a nonprofit corporation providing general systems, engineering, and integration support to Air Force space projects.

Despite her considerable accomplishments in the university sector, Estrin wishes she had had the chance to work in industry—an option that she says was not open to her in the earlier stages of her career. "The opportunities for women opened late for me," she says. "I've had a very satisfying career; I'm pleased with what I'm doing. But I wish I were 10 years younger and could move up a ladder of [corporate] responsibility. I like problem solving, and I like to deal with technical issues and the management of people [who will address] those issues. That was not much of a reality for me. If I hadn't gotten a PhD and gone into a university, I'd have had less opportunity."


*Wanda Garrett, analog applications engineer: "We get calls from customers who think we're secretaries. It's almost comical sometimes when we try to convince them that we can help them with their technical problems."*

**Filling in as role models**

Today, though the chances for women to move up the management ladder are somewhat improved, role models who can challenge the stereotyped views of men and women alike remain scarce. Dr Estrin recognizes her own value as a role model, and she believes her achievements benefited not only other women, but also the men with whom she worked. "By knowing me and having a good working relationship, they realized I was no different from them. And once you work with one woman, you stop thinking anything of it." Estrin has had the pleasure of witnessing how her work has helped lead to changes in some men's attitudes towards women engineers. "A number of men who told me about their daughter's interest in engineering have gotten in touch with me and told me that their daughters have gone into engineering and that they're very proud of them. That's a whole new group of men who are looking at women differently now."

Like Dr. Estrin, Wanda Garrett has seen how her presence has altered the attitudes of some of her colleagues. Shortly after she starting working for National Semiconductor, Garrett was asked to give a technical presentation along with a fellow worker. "He had serious doubts that I could carry it off," she says. "First, because I was young, and, second, because I was a woman. When it was over, he came over and told me he was glad that I had come along and that he thought the presentation had turned out very well."

Despite the salary gaps, the lingering stereotypes, and the obstacles to upper-level positions, many women in engineering say it is important to continue encouraging young women to enter the field, and to stick with it. To help young women who are beginning their careers, many of the women serve informally as role models for younger engineers at their companies. Gathright says several young women working as engineers at her company look to her for advice. "I think if I had had a role model and mentor, some of the trial and error would have been eliminated."

Many women also take time to represent engineering at career fairs for junior high school, high school, and college students. Preparation for an engineering career begins long before college. It really begins in junior high, where students' interest in science and math must be ignited so that, once they reach high school, they'll continue to take the courses that prepare them for collegiate studies. Through their contact with junior high and high school students, professional women hope to encourage the students to take upper-level math and science courses in high school so that their career options remain open.

At the college level, the women hope to reinforce engineering as a viable career option. Many young women who are interested in a science-based career may not have any idea of what an engineering job is like and may therefore steer away from engineering. The report by the Congressional Office of Technology Assessment cited a study that found 23% of first-year male students say they're interested in engineering, while only 3% of female freshmen are interested in engineering.

Barbara Mulkey, in fact, became interested in electrical engineering after attending a week-long introductory session to engineering that was sponsored by Purdue University. Because the session introduced her to career opportunities in which she could use her diverse interests in biomedicine, nuclear engineering, and the space program, she volunteered to participate in a similar session last year. "When I started [college], I had no idea what engineering was about," she says. "In high school, you take physics, biology, and chemistry, and you understand what jobs in those fields are. But until you get to college, you don't know what [engineering] classes are going to be about."

Stanford University has organized a mentor system to encourage women to pursue their interests in science and engineering careers. The program pairs undergraduate women with graduate and postdoctoral students having similar academic interests. Since it began last fall, the Women's Science and Engineering Network has enjoyed tremendous success. More than 330 female undergraduates signed up as participants, and nearly 100 graduate and postdoctoral students signed up to act as advisors. In addition to the student advisors, the network includes advisors from among the faculty and from IBM and Hewlett-Packard.

Concern about maintaining increased enrollments of women in engineering programs has been expressed in recent reports from the National Academy of Sciences, the National Science Foundation, and the Commission on Professionals in Science and Technology. The report from the Congressional Office of Technology Assessment cited stereotyped career expectations and differential treatment of women who work as scientists and engineers as the major factors discouraging women from entering these fields. Despite these limiting factors, the report stated optimistically that "there appears to be no inherent reasons why these increases [in women's participation in engineering] should not continue."

There is also a much more practical reason why education and industry must continue to emphasize opportunities for women in engineering, says Shirley Malcolm. That reason is technological advancement. "What nation," she asks, "no matter how rich it is, can afford to waste the talents of well over one-half of its population?"

**EDN**

*Part 2 of this series will appear in the May 29 section of Professional Issues.*

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# CAREER OPPORTUNITIES

## 1986 Editorial Calendar and Planning Guide

| Issue Date | Recruitment Deadline | EDN Editorial Emphasis | EDN CareerNews |
|---|---|---|---|
| June 12 | May 21 | Digital Technology Special Issue; Personal Computer Boards; Development Systems (CAE-related*); Computer ICs; NCC Show Preview | Closing: 6/19 Mailing: 6/30 |
| June 26 | June 5 | CAE Systems; Communications ICs; Military Microcomputers; Semicustom IC Design (CAE-related*) | |
| July 10 | June 19 | Product Showcase—Volume I; IDs & Semiconductors; Hardware & Interconnection Devices; Power Supplies/Sources; Software; Literature on Computers & Peripherals, Components, Test & Measurement Instruments, International Products | |
| July 24 | July 2 | Product Showcase—Volume II; Computers & Peripherals; Components; Test & Measurement Instruments; International Products; Literature on ICs & Semiconductors, Hardware & Interconnection Devices, Power Supplies/Sources, Software | |
| Aug. 7 | July 17 | Resistors; CAE; Communications ICs; Microprocessor Development Software; Technical Article Database Index | Closing: 8/14 Mailing: 8/26 |
| Aug. 21 | July 31 | Military Electronics Special Issue; High-speed ICs; Communications Technology | |
| Sept. 4 | Aug. 14 | Test & Measurement Special Issue; Oscilloscopes; Automated Design & Engineering for Electronics Product Preview (CAE-related*); Meters; Display Technology | Closing: 9/11 Mailing: 9/23 |
| Sept. 18 | Aug. 27 | Personal Computer-Based CAE; Power ICs; Computer Peripherals; Hardware & Interconnection Technology; EDN 30th Anniversary Tribute | |
| Oct. 2 | Sept. 11 | Surface Mount Technology; Memory ICs; CAE; Semicustom IC Directory (CAE-related*) | Closing: 10/16 Mailing: 10/28 |
| Oct. 16 | Sept. 25 | Digital Signal Processing; Personal Computers; ICs; Test & Measurement Instruments; Display Technology | |
| Oct. 30 | Oct. 8 | Batteries; Converters; Wescon '86 Product Preview; European Electronics; Computer Boards | |
| Nov. 13 | Oct. 23 | Wescon '86 Show Issue; Op Amps; CAE; Semicustom ICs (CAE- related*); Artificial Intelligence (CAE-related*) | Closing: 11/3 Mailing: 11/25 |
| Nov. 27 | Nov. 6 | Microprocessor Technology Report & Directory; CAE; Passive Components | |
| Dec. 11 | Nov. 18 | Product Showcase—Volume I; ICs & Semiconductors; Hardware & Interconnection Devices; Power Supplies/Sources; Software; Literature on Computers & Peripherals, Components, Test & Measurement Instruments, International Products | |
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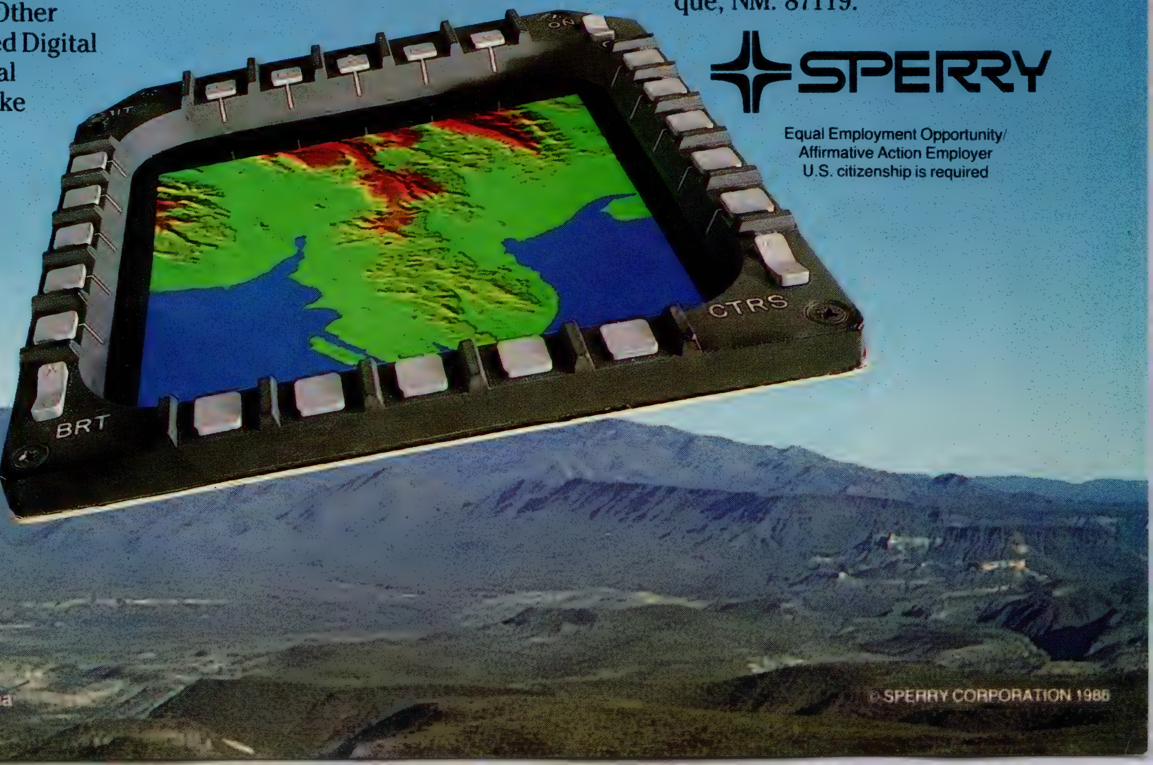


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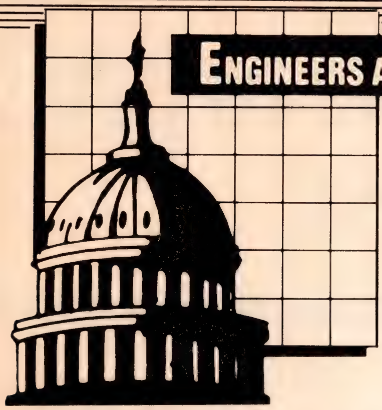

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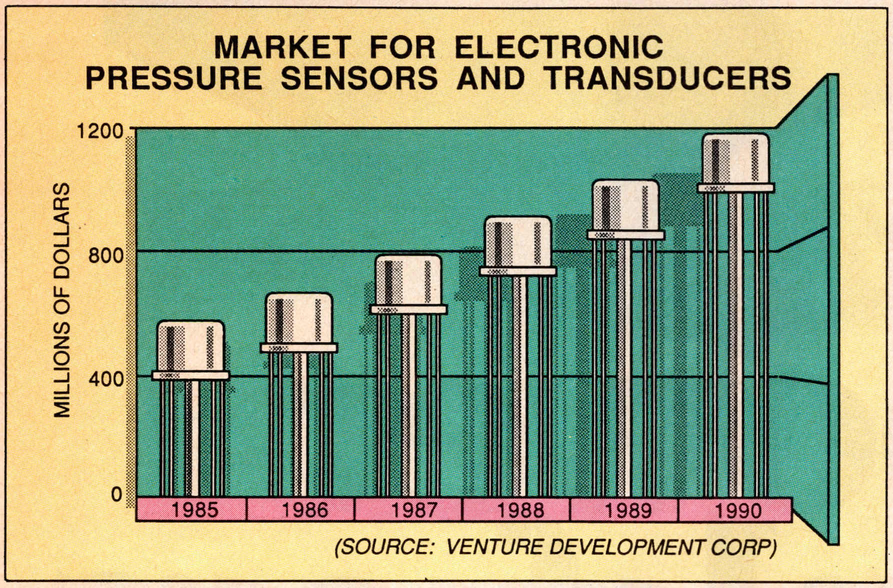


## Pressure-transducer demand continues rapid growth rate

Over the next five years, the demand for pressure sensors and transducers will double, according to Venture Development Corp (VDC), a market-research company in Natick, MA. The value of shipments in 1985 was $573 million, and according to VDC, will be near $1.2 billion in 1990. This growth rate reflects a continuation of strong demand for electronic pressure-sensing devices, which commanded a $183 million market in 1978.

Electronic pressure sensors and transducers convert the pressure value of a variety of media—gas, liquid, etc—into an electronic signal that's proportional to the measured pressure. Manufacturers use a number of technologies to effect the conversion mechanism, including strain-gauge, variable-capacitance, LVDT (linear variable differential transformer), potentiometric, vibrating-wire, and piezoelectric techniques (see Special Report, "Pressure Sensors and Transducers," EDN, May 1, pg 100).

Of these methods, piezoelectric strain-gauge types are subject to the most recent innovation. Semiconductor manufacturers are diffusing the strain-gauge bridges onto silicon, and they're able to integrate other components to add signal-conditioning functions, amplification, and—just recently—μPs and memory. The manufacturers are also maintaining the IC-based-device performance levels customers have come to expect, as well as reducing prices.

Although innovations that allow the production of "intelligent," digital devices will help bring pressure sensors and transducers to manufacturing environments, VDC believes that devices with digital output signals are not likely to gain popularity until suitable standards, like General Motor's Manufacturing Automation Protocol, have been defined and accepted and become economically feasible.

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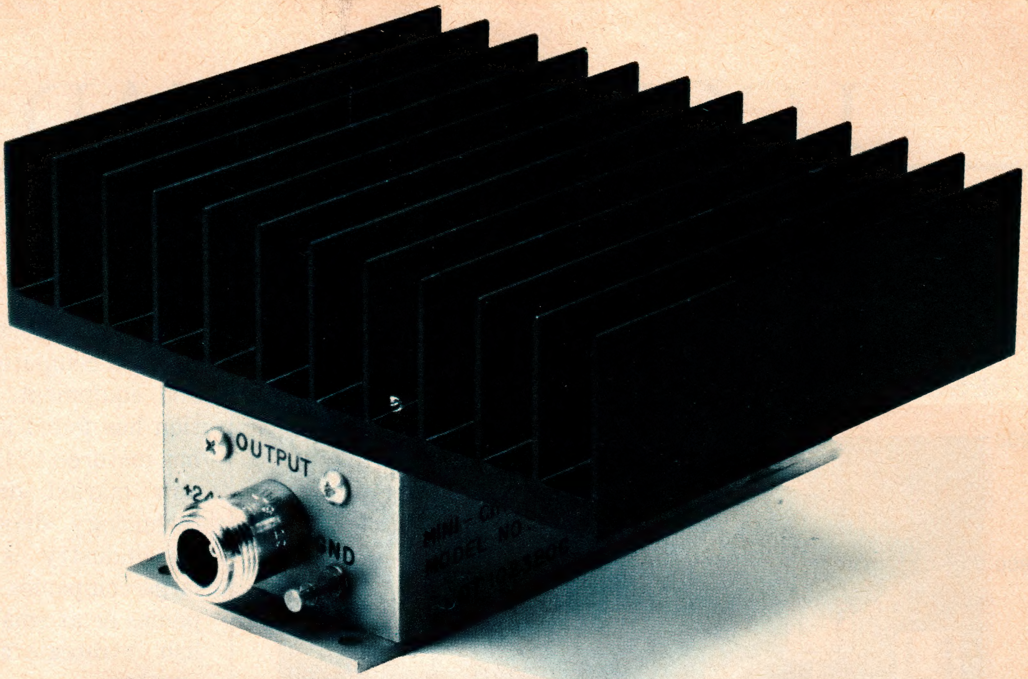
## Demands catch technology in computer-graphics market

In an effort to chart the future of computer graphics systematically, the National Computer Graphics Association (Fairfax, VA) has recently attempted to list and assess the trends affecting users and suppliers of computer-graphics systems and equipment. What the association has found is that the industry has matured to the point where it is now market driven rather than technology driven. Furthermore, the industry is consolidating, as large companies acquire small companies or as small companies establish "strategic alliances" with one another.

According to the NCGA, many users are becoming more sophisticated. They're less likely to be dazzled by the technology and more likely to consider computer graphics as a solution to a particular problem. In addition, the increasing use of computer graphics by nontechnical users shows that organizations are integrating graphics systems and usage with other day-to-day operations, and that computer graphics is less often perceived as an isolated tool.

In terms of technology, developments are now more evolutionary than revolutionary, reports the NCGA. Other technology trends are becoming evident:

- Adoption of standards is reducing the diversity of products.
- Soon there will be no "holes" across product lines, eg, low-cost printers and plotters will accommodate the output of systems with very high resolutions.
- Users are showing a greater need for better software than for better hardware.
- Laser technology will be one of the most important ancillary technologies, particularly in scanning devices and color hard copy.
- Telecommunications and networking are becoming increasingly important elements of computer-graphics products.

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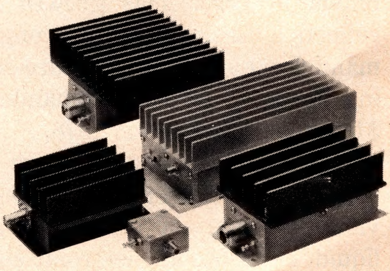

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